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ACC-25-002
29 December 1982

(1)

FINAL DOCUMENTATION OF AN ENHANCED ROBUSTNESS MODULE DESIGN (Reference ACC Maintenance Manual for Robustness II)

Submitted to: Defense Advanced Research Projects Agency
Information Processing Techniques Office
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Submitted by: Associated Computer Consultants
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B071074 Alma.

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1400 WILSON BOULEVARD
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JAN 21 1983
Jan 21, 1983

Contracting Officer
Associated Computer Consultants
720 Santa Barbara Street
Santa Barbara, CA 93101

Dear Sir:

Reference is made to ACC-25-002, Final Report-Robustness II Maintenance Manual," dated 29 December 1982 produced under AO 4024, Contract MDA 903-82-C-0478, which is approved for publication as Unclassified.

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ROBUSTII.MM.V001
December 1982

ROBUSTNESS II

MAINTENANCE MANUAL

Table of Contents

CHAPTER 1

1.0 INTRODUCTION

1.1 Maintenance Manual Contents - This manual describes the hardware, application, operation, and maintenance of the Robustness II Module (ACC Part #8100133) manufactured by Associated Computer Consultants, Santa Barbara, California.

1.2 Maintenance Manual Organization - This manual is divided into five chapters as follows:

Chapter 1 - Introduction
Chapter 2 - References
Chapter 3 - Physical Description and Installation
Chapter 4 - Address Selection, Programming, and Option Selection
Chapter 5 - Drawings, Parts List, Schematics

1.3 Robustness II Module Overview - The Robustness II Module consists of one dual-width printed circuit assembly as shown in Figure 1-1. It was designed to enhance the Digital Equipment Corporation (DEC) LSI-11 family of computer systems. Operating on the LSI-11 bus (Q-bus) as shown in Figure 1-2, the Robustness II provides features required by systems operating on telecommunication networks.

1.4 Robustness II Module Application - The Robustness II Module provides a number of functions on a single module in order to allow the programmer great flexibility in system implementation while consuming a minimum of I/O space.

1.4.1 On-Board Boot Code Space - The programmer can use the Robustness II Module to implement onboard boot code to start or restart programs automatically. The Robustness II is available with 4K or 8K words of EPROM, which take only two Q-bus address spaces. This allows operating system software to be stored in EPROM for downline loading rather than on disk or tape. By use of additional dual-width Memory Expansion Boards, which can be attached to the Robustness II Module, additional program storage is available.

1.4.2 Manual Switch Registers - Four switch registers (64 bits) are provided to allow the programmer to store semi-permanent (non-volatile) information such as system I.D., operational function configuration, or system address.

1.4.3 Elapsed Time Counter - For applications in which timing must be checked, a 10KHz counter/timer is provided that can be read at the start and finish of an operation to give an accurate account of the elapsed time during operation.

1.4.4 Watchdog Timer - A Watchdog Timer is provided to restart the system if the Watchdog Timer Register is not "written" every six seconds (or another of seven selectable timeout periods). At a power or software failure, the Watchdog Timer times out and reboots the system. This timer can be disabled for maintenance or software development by setting a switch. It cannot be accidentally disabled under software control.

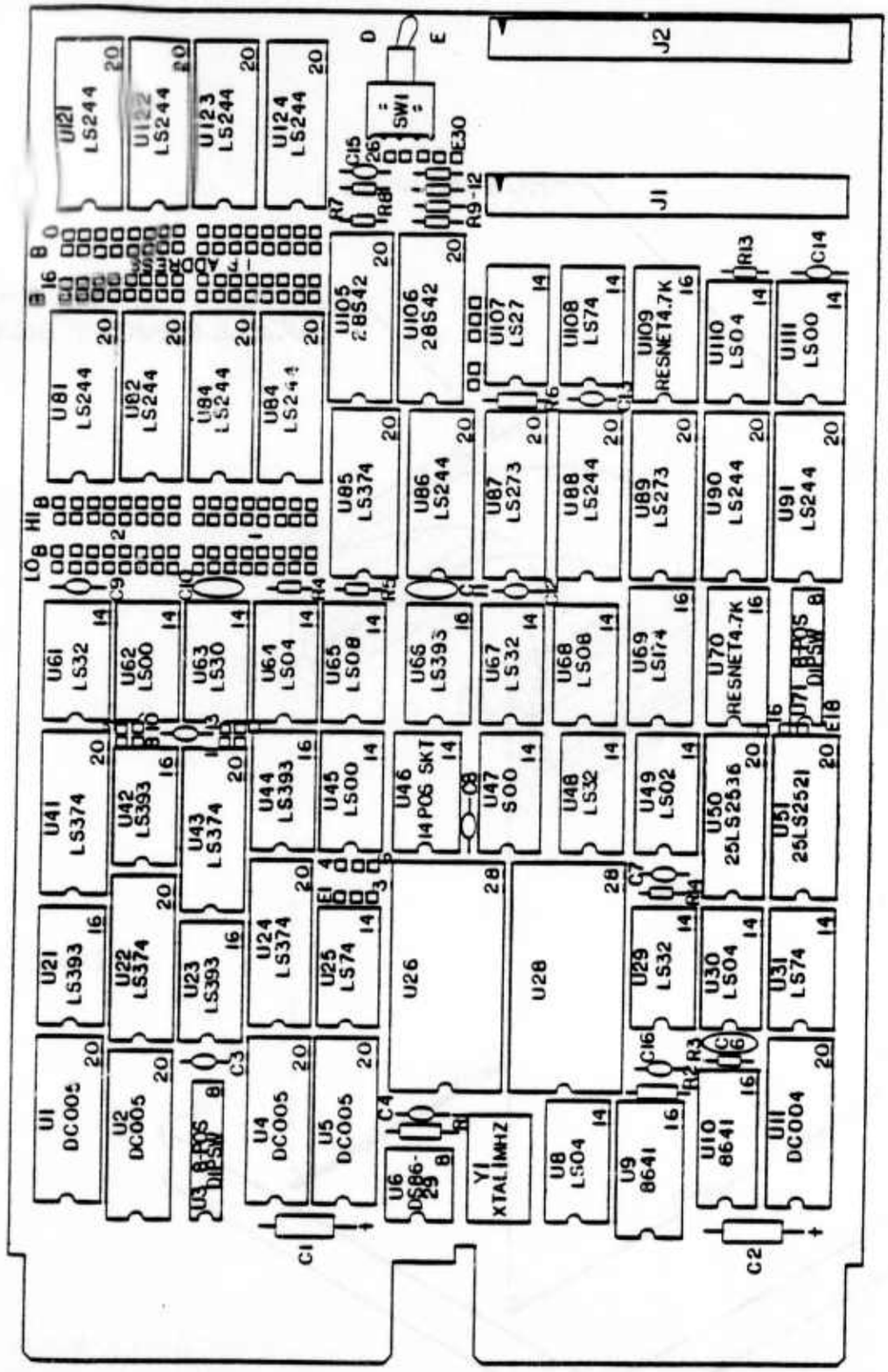


Figure 1-1 Robustness II Module

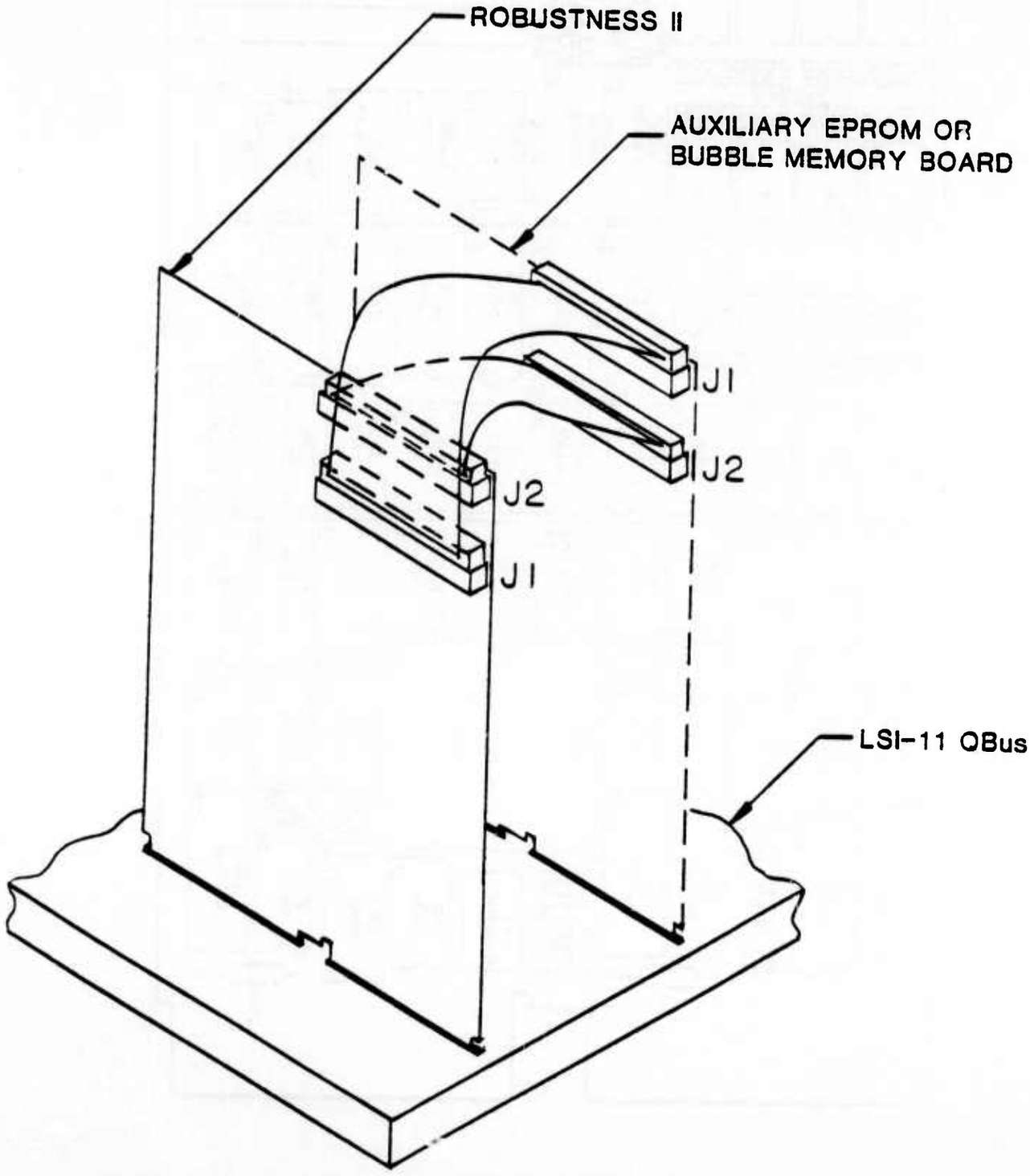


Figure 1-2 LSI-11 Backplane With Robustness II

CHAPTER 2

2.0 REFERENCES

2.1 Reference Documents - The following documents contain additional information on the Robustness II Module.

1. The TTL Data Book
   Texas Instruments Incorporated

2. Interface Data Book
   National Semiconductor Corporation

3. The Bipolar Microcomputer Components Data Book
   Texas Instruments Incorporated

4. The MOS Memory Data Book
   Texas Instruments Incorporated

5. Microcomputers and Memories
   Digital Equipment Corporation

6. Microcomputer Interfaces Handbook
   Digital Equipment Corporation

7. Schottky and Low-Power Schottky Data Book
   Advanced Micro Devices, Incorporated

CHAPTER 3

3.0 PHYSICAL DESCRIPTION AND INSTALLATION

3.1 Robustness II Module Particulars - The Robustness II Module is a dual width printed circuit board as shown in Figure 1-1. It is connected to the LSI-11 bus (Q-bus), and requires one standard load to that bus. Though the Robustness II Module does not use interrupts or DMA transfers, it does provide grant continuity for interrupts and for DMA grant signals. The Robustness II Module consumes approximately 2.5 Amperes at +5Vdc. No other voltages are required.

3.2 External Cabling - Two connectors (J1 and J2) are provided for external cable connection to the Robustness II Module. See Figure 2-1 for an illustration of this interconnection.

3.3 Robustness II Module Organization - The Robustness II consists of three main sections which are listed below and explained in the subsequent paragraphs.

Boot PROM Section
Registers/Watchdog Timer
External Bus

3.3.1 Boot PROM Section - The two boot PROMs contain a total of 512 words (512x16 bits) of PROM. Because of the address space limitations of the LSI-11 bus I/O page, only a portion of this PROM space is used at any one time. Two configurations for PROM use are available: 256 words of PROM or 128 words of PROM. With the 256 word configuration, either of the 256 word blocks may be selected by wire wrap jumpers. In the 128 word configuration, any one of the four 128 word blocks may be selected by wire wrap jumpers. These configurations are discussed in detail in Chapter 4. The actual I/O page address of the PROM block can be set by the user.

3.3.2 Register Section - The Register Section contains eight (word) registers that provide most of the Robustness II Module functions. The base address of this block of registers in the I/O page can be set by the user (see Section 4.1). The registers listed below are described in Chapter 4.

00 Control/Status Register
02 Cell Address Register
04 Data Register
06 Timer/Counter Register (least significant word)
10 Timer/Counter Register (most significant word)
12 Switch Register No. 1 (read) Watchdog Timer (write)
14 Switch Register No. 2
16 Not Used

3.3.3 External Bus - External bus connections J1 and J2 are provided to connect up to 256K words of external RAM, ROM, PROM, EPROM or Bubble memory. All incoming control signals provide open collector inputs to allow more than one external bus connection at a time. Figure 1-2 illustrates the interconnection of memory extension boards to the External Bus.

CHAPTER 4

4.0 ADDRESS SELECTION, PROGRAMMING, AND OPTION SELECTION

4.1 Robustness II Register Block Address Selection - The register block address is controlled by the eight DIP switches on U03 and one DIP switch on U71. Figure 4-1 shows the DIP switches on U03 and U71 and the associated address line of each. The address block selected must not interfere with that of an already existing device on the LSI-11 bus. When a DIP switch is closed, the associated address line must be asserted for a match. When a DIP switch is open, the associated address line must be negated for a match. All switch settings must match their appropriate address lines before the register bank can be selected.

4.2 Control/Status Register (CSR) - This register provides status and control to the other Robustness II registers, the external bus interface, and the boot PROM section. The following table describes each of the CSR bits. These CSR bits are referred to in discussions of the other registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	ø
Error	Invalid Address	Not Write Enabled	Not Written	Not Used	Watch Dog Is Disabled	BD2 Can Write	BD2 Is There	All OK	Boot Select	Switch Bank Enable	BD2 Write Enable	Ext. Addr Bit 17	Ext. Addr Bit 16	Board 2 Select	Timer Latch Enable
R	R	R	R	-	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	W

W = Write Only
R = Read Only
R/W = Read or Write

BIT	DEFINITION
0	Timer/counter Latch Enable - Latches the 32 bits of the counter/timer into the two counter/timer registers.
1	External Bus Select - Sets the external bus enable line on the external bus. Also disables on-board EPROM and enables the error bits 12, 13, and 14 to indicate errors from the external bus rather than from the Robustness II Module.
2	Extended Address Bit 16 - Used by the external bus to extend the addressing capability of the 16 bit cell address bus (CELADR00 - 15).
3	Extended Address Bit 17 - Used by external bus to extend the addressing capability of the 16 bit cell address bus (CELADR00 - 15).
4	Board 2 Write Enable - A high (1) sets the write enable line on the external bus. A low (0) acts as a write protect for the external bus.
5	Switch Register Bank Enable - A low (0) enables Bank A of both switch registers and a high (1) enables Bank B.

6 Boot Select (if wire-wrapped into the PROM boot addressing) - Selects one boot PROM block or another.

7 All OK - Indicates that the Robustness II module is functioning, and that the external bus is functioning if it is selected.

8 External Bus is There - Incoming signal line from external bus asserted (high) indicates that there is a board connected to the external bus.

9 External Bus Can Write - Incoming signal line from external bus bus asserted (high) indicates that the board connected to the external bus is writeable.

10 Watchdog Timer Disabled - An active low (0) signal Watchdog Timer Disabled - An active low (0) signal indicates that the watchdog timer has been disabled by switch 1 on the Robustness II card edge.

11 Not Used

12 Address Not Writeable - An error bit. When asserted (high) indicates that a write was tried to read only memory. Any write to the Robustness II EPROM will cause this error. An error of this type from the external bus is possible but indication of the error depends on the external bus configuration to so indicate.

13 Address Not Write Enabled - An error bit. When asserted (high) indicates that a write was tried 1) to the Robustness II EPROM, or 2) to the external bus while CSR bit 2 (external bus write enable) was negated.

14 Invalid Address for Robustness II - When asserted (high), indicates that the given address is out of range of the EPROM (either 4K or 8K words selected). When the external bus is selected and CSR bit 2 is asserted (high), an error signal from the external bus (BD2BAD) asserted (high) will also assert this error bit.

15 Error - Master error bit. Logical OR of CSR error bits 12, 13, and 14.

4.3 Cell Address/Data Register - The Robustness II module supports either 4K or 8K words of board EPROM memory. This memory is accessed through two registers, the Cell Address Register (address XX02) and the Data Register (address XX04). To read a block of memory, the programmer loads the starting address into the Cell Address Register, then reads the Data Register. To access the next word, the Cell Address Register is loaded with the next word address and the Data Register is again read. Unlike a standard bus address, the Cell Address Register addresses words only, so the first word is at address 0 (octal), the next at address 1, then 2, 3, 4, and so on. See 4.3.1 and 4.3.2 for details.

4.3.1 Cell Address Register - The cell address register is a 16 bit read/write latch. When written to, this register latches the 16 bit word of address information onto the cell address bus (CELADR00 - 15). This address word selects one data word, which is placed on the BDA bus when the data register is read. The address word is used by the onboard EPROM (CELADR00 - 11), or by the external bus (CELADR00 - 15) if it has been selected. The cell address register is configured for word addressing only. The least significant bit of the cell address bus (CELADR00) indicates low word/high word, not low byte/high byte. This configuration extends the 18 bit address range to 256K words, from the normal 256K bytes usually accessable by an 18 bit address. A block of data can be consecutively read by continually updating the cell address register with the address of the next word of data, and then reading the cell data register.

4.3.2 Data Register - There is no actual hardware data register. The address information latched onto the cell address bus (CELADR00 - 15) selects the memory word, and a read or write to the cell data register performs a read or write to or from the selected memory word. Since the memory word is tri-stated (buffered) onto the BDA bus, an actual hardware data register is not necessary.

4.4 The Timer/Counter Registers 1 and 2 - The 32 bit timer/counter runs continuously at 10KHz and can be latched into the two timer/counter registers at any time by ORing a 1 into CSR bit 0. Then the registers can be read at the programmer's leisure. The least significant word is at address XX06, and the most significant is at address XX10. An event can be timed by latching the timer/counter registers, starting the event, and then reading the registers to get the starting time. When the event is completed, the timer/counter registers are again latched, and the first reading is subtracted from the second to give the elapsed time in 10KHz increments. This may be converted to a more convenient format, such as minutes, seconds, tenths and hundredths, as required.

4.4.1 Details of Timer/Counter Registers 1 and 2 - The 32 bit timer/counter uses a 10KHz clock, which is derived from a 1 MHz crystal oscillator. A one written to bit 0 of the CSR latches the 32 bits of the timer/counter, in two 16 bit halves, into timer/counter registers 1 and 2 where they can be read. The 32 bits are latched so that one 16 bit half does not increment into the next between reads and cause a false reading. Timer/counter register 2 contains the most significant 16 bits.

4.5 Watchdog Timer - The watchdog timer is provided as a watchdog to the system. If the system fails to reset the watchdog timer for any reason, the watchdog timer will reinitialize the system. The watchdog timer is reset by writing a 370 or 371 (octal) to address XX12 of switch register 1 before the timeout period has expired. The timeout period is factory set at approximately six seconds, but may be changed as explained in chapter 4. The watchdog timer may be disabled by setting switch 1 to the D position. When the watchdog timer is enabled, CSR bit 10 is asserted (1); when disabled, CRS bit 10 is negated (0).

4.5.1 Details of Watchdog Timer - The Watchdog Timer will restart and reboot the CPU if the program in control fails to reset the timer by writing 370 or 371 (octal) into the Watchdog Timer Register. This ensures that hardware or software interruptions to proper program flow do not disable the system for any longer than one watchdog timeout period (factory set at 6 seconds). The timeout period can be changed by the user to accommodate other programming environments. The Watchdog Timer can be disabled by setting switch 1 to the D (disabled) position.

NOTE

The Switch Register 1 (see 4.6) and Watchdog Timer Register functions are performed by one dual function register. A read of this register will provide the contents of Switch Register 1. A write of the correct code to this register will reset the Watchdog Timer.

4.6 Switch Registers 1 and 2 - The two 16 bit switch registers will access a total of 64 bits of information through bank selection. Switch register 1 will read Bank A1 (16 bits) and Bank B1 (16 bits), while switch register 2 will read Bank A2 (16 bits) and Bank B2 (16 bits). Bank selection is enabled by CSR bit 05. A low (0) selects Bank A, and a high (1) selects Bank B. Each of the bits is a wire wrap stake pair that, when wrapped, equals a low (0), and when unwrapped, equals a high (1).

4.7 External Bus - The external bus consists of an address bus (CELADR00 - 15, and CSR bits 2 and 3 for extended address lines 16 and 17), a data bus (BDA00 - 15), and a control bus (including CSR bit 01, external bus enable). Any number of external devices may be connected to the external bus. All of the incoming control lines are pulled up and are designed for open-collector (wired-OR, active low) connection of a number of boards. A total of 256K words of any type of memory may be connected. RAM, ROM, EPROM, EEPROM, or Bubble memory can be connected using the available control signals.

4.8 Configuration of Options - The following options are wire-wrap selectable by the user and are discussed in the paragraphs that follow. A directory of wire wrap locations is given in Figure 4-2.

- EPROM Memory Space
- Address out of Range Error
- Watchdog Timer
- Counter/Timer Reset
- Switch Register Wiring

4.8.1 EPROM Memory Space - The Robustness II Module provides the option of either 4K or 8K words of onboard EPROM. Figure 4-3 shows the installation of 4K words of EPROM (2532) and the associated 4K wire wrap jumper. For the 4K installation, pin 1 of the 24 pin 2532 EPROM must be inserted in pin 3 of the 28 pin EPROM socket. Figure 4-4 shows the installation of 8K words of EPROM (2564) and the associated wire wrap jumper.

4.8.2 Address Out of Range Error - CSR bit 14 (INVADR) indicates an address that is out of range for the onboard 4K or 8K word EPROM. The address limit has a default setting of 4K words, but may be changed for 8K words. The procedure to change the address limit is shown in Figure 4-5.

4.8.3 Watchdog Timer - The watchdog timer reinitializes the system if it is allowed to time out. It can be disabled by setting switch 1 to the D position. As set, the watchdog timer will time out after approximately 6 seconds. This timeout period can be changed by changing the input clock frequency. There are eight clock frequencies available. Figure 4-6 shows how to cut the existing trace and wire wrap the selected clock frequency (time) to the input of the watchdog timer.

4.8.4 Counter/Timer Reset - The counter/timer runs continuously and is normally reset only on system initialization. An optional input is available that allows the user to wire a reset switch into the counter timer reset circuit. This allows the user to reset the counter/timer switch by pushing a button. Figure 4-7 shows the connecting points for a user supplied switch.

4.8.5 Switch Register Wiring - The configuration for the 64 bits of the switch registers is shown in Figure 4-8. Each of the 64 bits has a pair of wire wrap stakes designed to install a jumper clip. If the clip is installed, that bit will read as a zero (0). If the clip is left off, (open), the bit will read as a one (1).

4.8.6 Boot PROM Block Address - The boot PROM block starting address is selected by switches 3 through 7 on U71. Figure 4-9 shows how to set the switches for the address selected.

4.8.6.1 Boot PROM Block Size - The boot PROM block size is selectable as either a 128 word or 256 word block. Figure 4-10 shows how to set both configurations.

4.8.6.2 Boot PROM Configuration - The Robustness II contains two 28S42 PROMs. These PROMs are 512 X 8 bits each in low byte-high byte parallel, and provide 512 16 bit words of PROM. The PROMs can be configured in either 128 or 256 word blocks, and the blocks may be either fixed or switched under software control. Figures 4-11 and 4-12 show the possible configurations and the wire wrap jumper configurations for each.

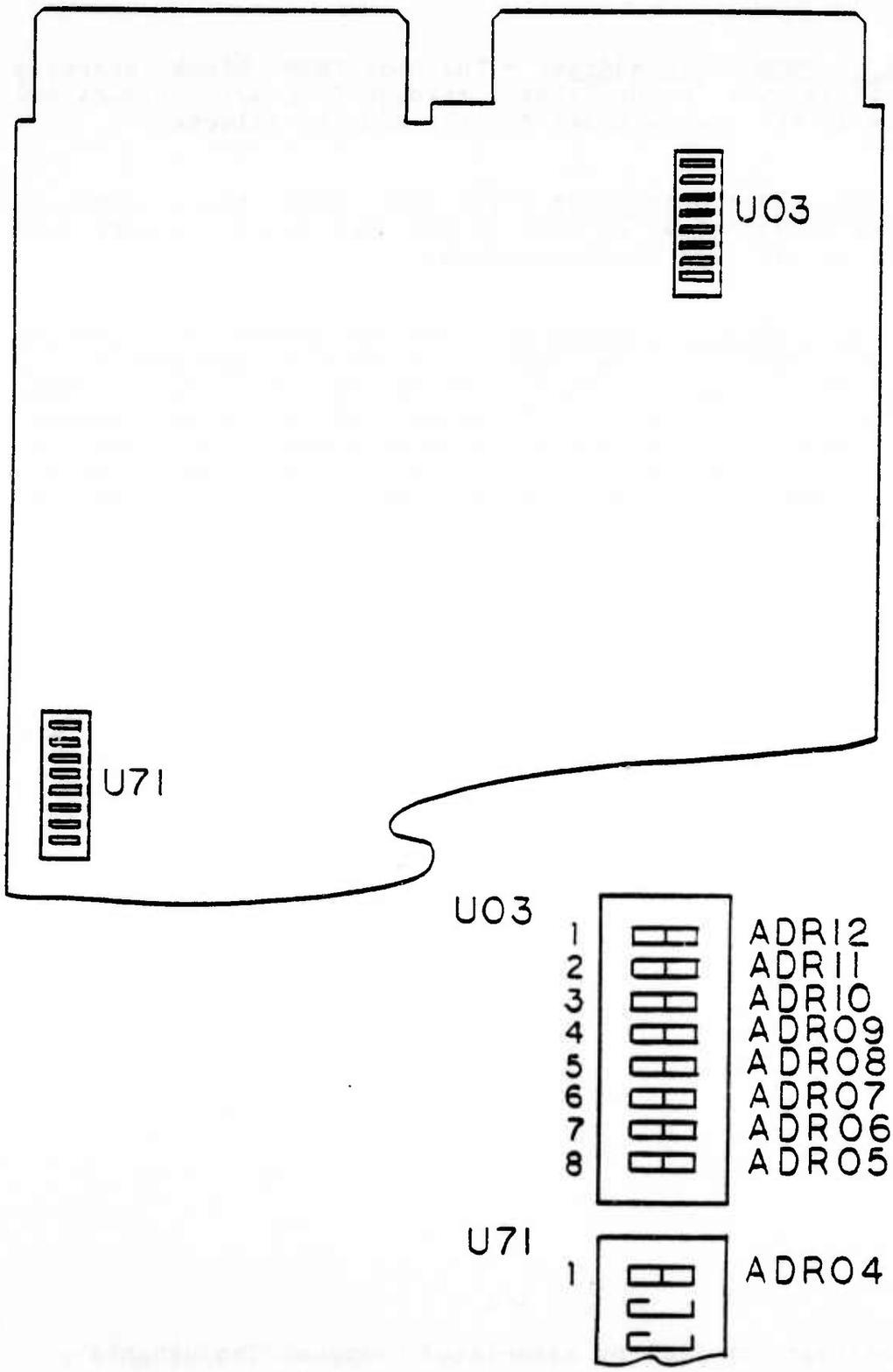
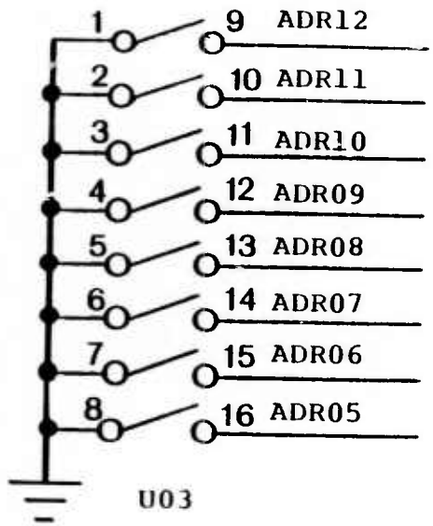
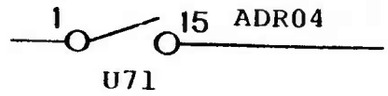


Figure 4-1. Robustness II Register Block Address Selection (Sheet 1 of 2)





	7			7			5			0			0			0		
Register Block Address	17		15		13		11		9		7			5		3		1	
		16		14		12		10		8		6			4		2		0
Address in Binary	1	1	1	1	1	1	1	0	1	0	0	0	0		0	0	0		0
Register Block Switch Settings	X	X	X	X	X	C	C	0	C	0	0	0	0		0	X	X	X	X

X = Don't Care
C = Closed
0 = Open

Figure 4-1. Robustness II Register Block Address Selection (Sheet 2 of 2)

E-POINT	SIGNAL	FIGURE NUMBER
E1	CELADR12	4-3
E2	2532 EPROMS, PIN 23 (VPP)	4-3
E3	VCC	4-3
E4	TLATCH OUT	4-13
E5	TLATS	4-13
E6	TLATCH IN	4-13
E7	TMR00	4-6
E8	TMR10	4-6
E9	TMR09	4-6
E10	TMR11	4-6
E11	TMR04	4-6
E12	TMR06	4-6
E13	TMR05	4-6
E14	TMR07	4-6
E15	TMR08 - TO WATCHDOG TIMER	4-6
E16	BDA08	4-10
E17	U71, PIN 10 (MAT08)	4-10
E18	U51, PIN 14 (MAT09)	4-10
E19	NOT USED	
E20	GND	4-5
E21	U107, PIN 11, GND	4-5
E22	CELADR12	4-5
E23	U107, PIN 10	4-5
E24	BRESET-	4-7
E25	GND	4-7
E26	U85, PIN 2, ROM08A	4-11, 4-12
E27	ROM08, U105, U106	4-11, 4-12
E28	GND	4-11, 4-12
E29	VP	4-11, 4-12
E30	BD2SEL	4-11, 4-12
E31	WRDOUT (U65, PIN 11)	4-14

Figure 4-2. Robustness II Wire-Wrap Locations (Sheet 1 of 2)

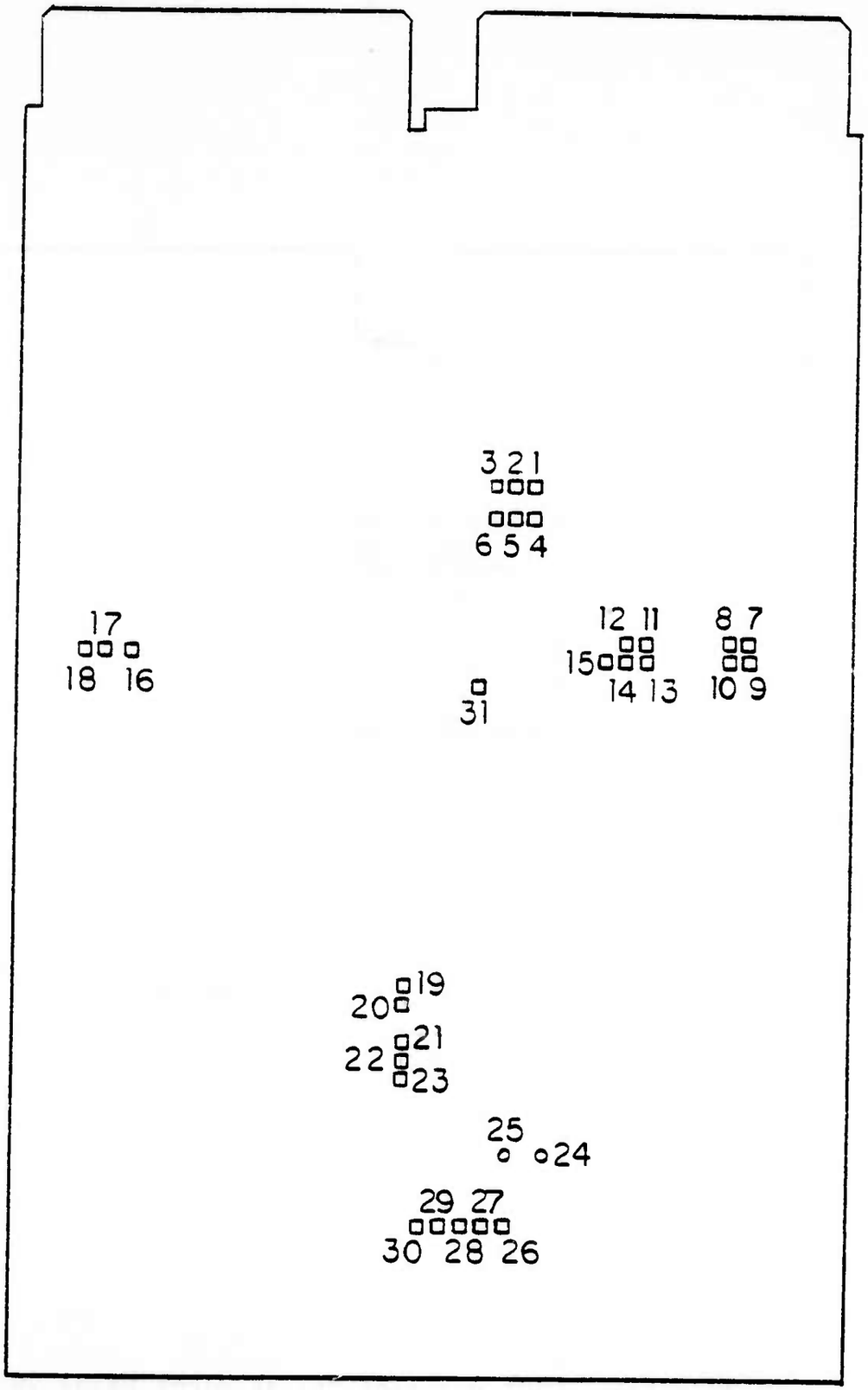


Figure 4-2 Robustness II Wire Wrap Locations (sheet 2 of 2)

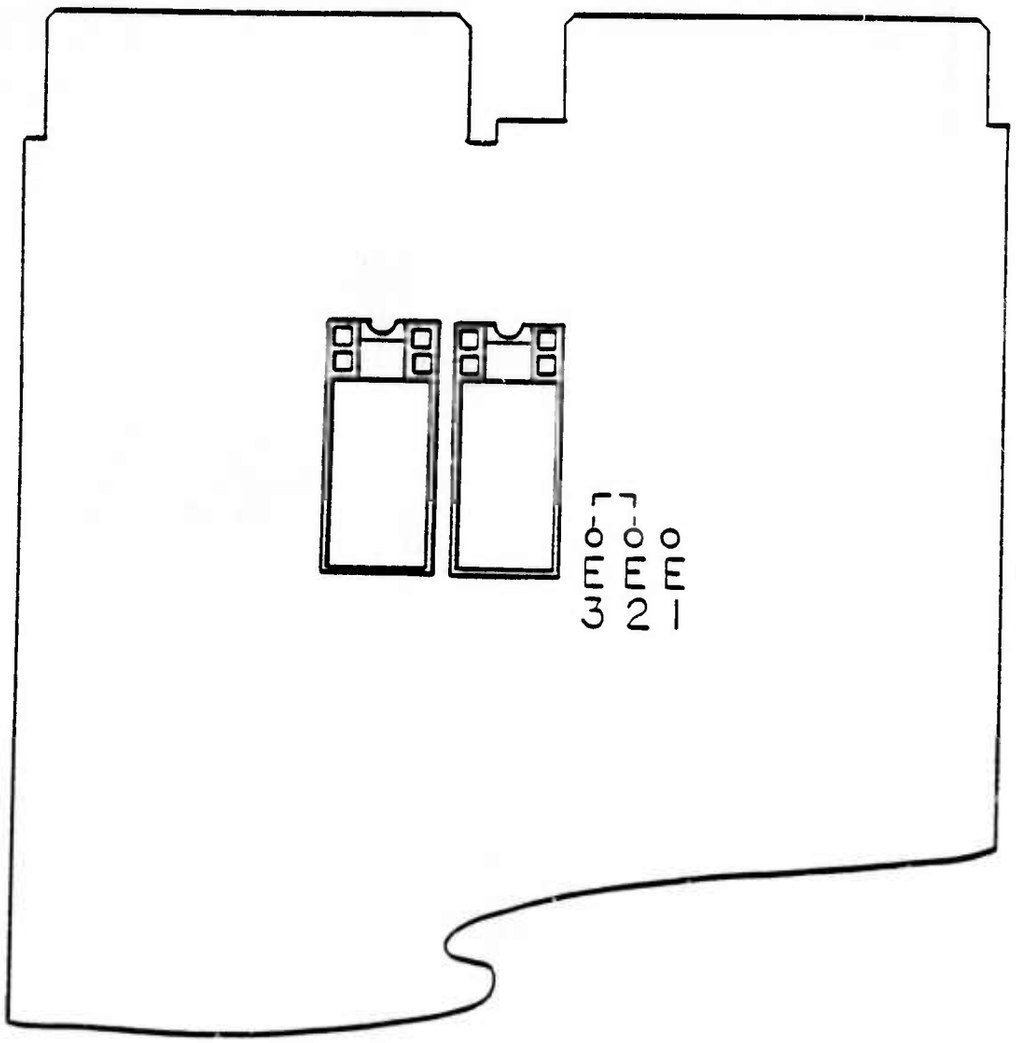


Figure 4-3 Configuration for 4K Words Using 2532 EPROMs

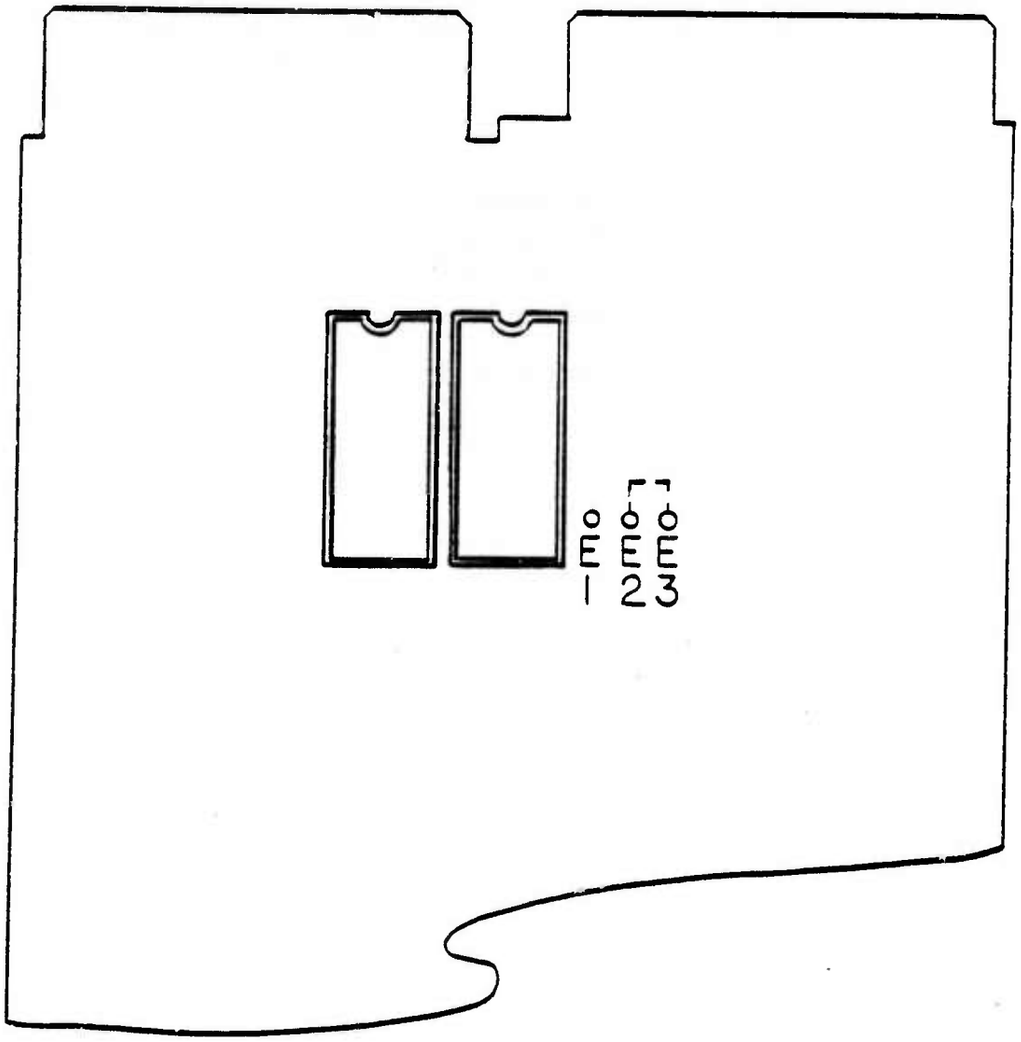
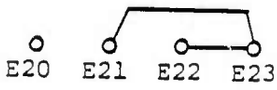
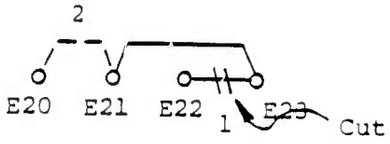


Figure 4-4 Configuration for 8K Words Using 2564 EPROMs.



On Board Address Range Check

Wire Wrap for 4K Words EPROM (Factory Wired)



On Board Address Range Check

Wire Wrap for 8K Words EPROM (User Wired)

1 Cut the trace on layer 6 (solder side of board) between E22 and E23

2 Add a wirewrap jumper between E20 and E21

Figure 4-5

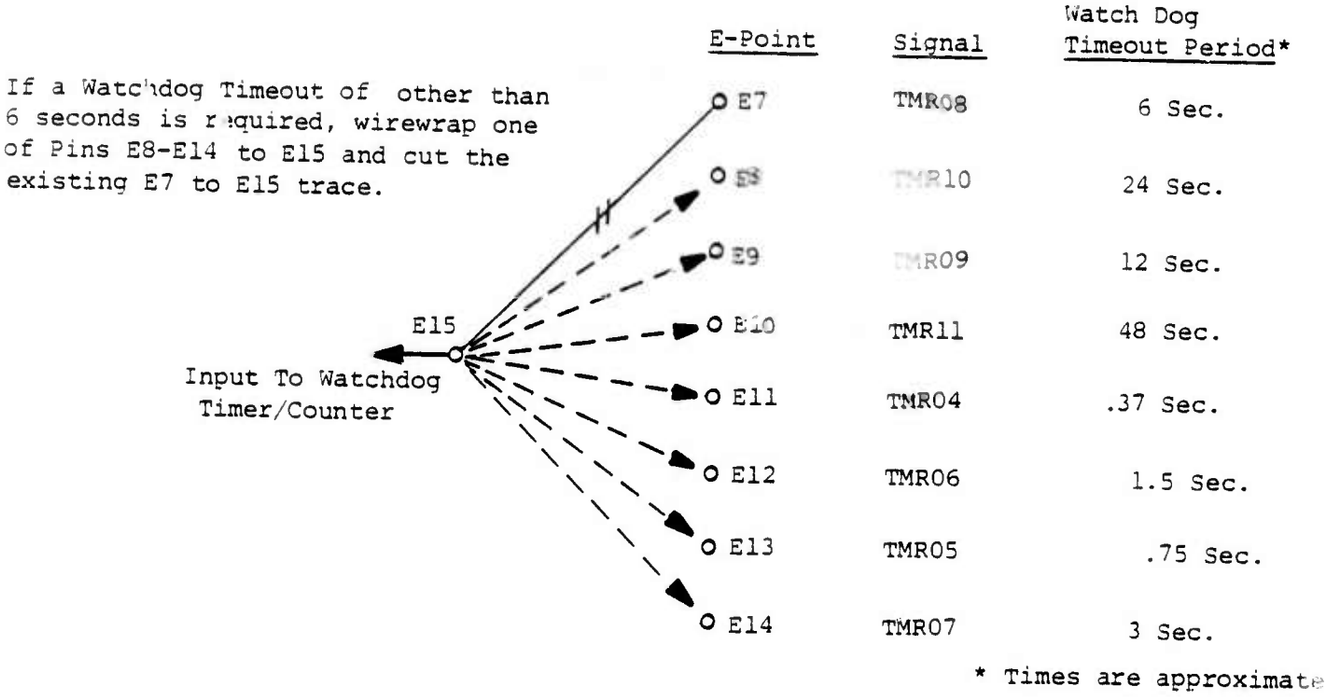
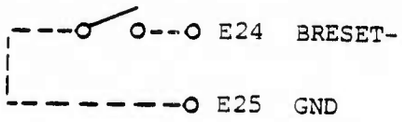


Figure 4-6 Watchdog Timer Counter Input Select



Off Board Switch connected by the
User to reset the counter/timer to zero.

Figure 4-7

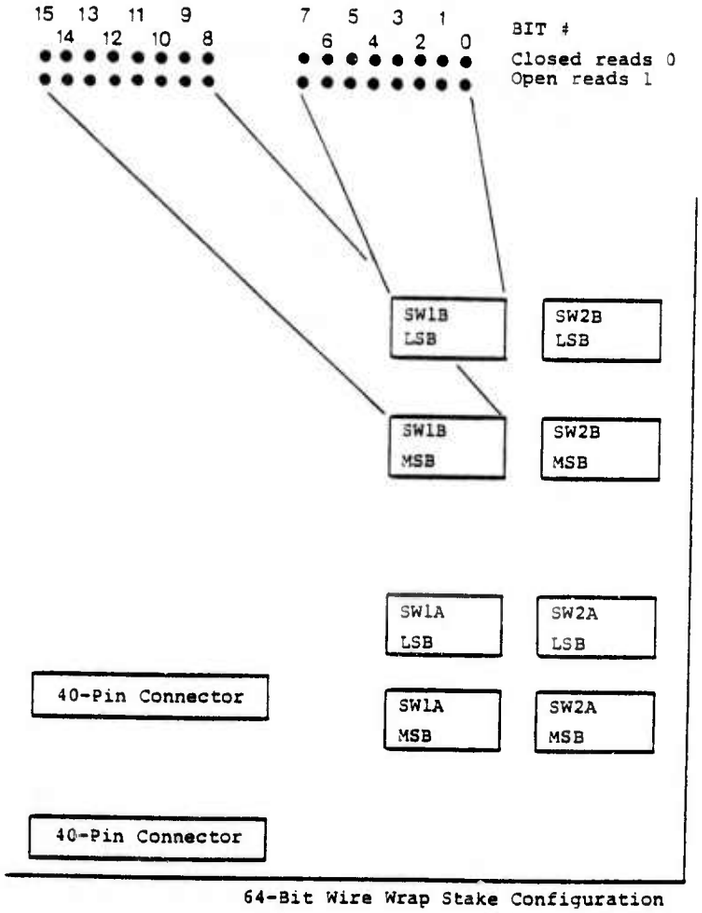
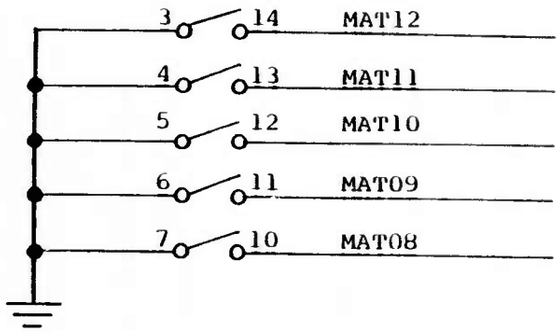


Figure 4-8

U71

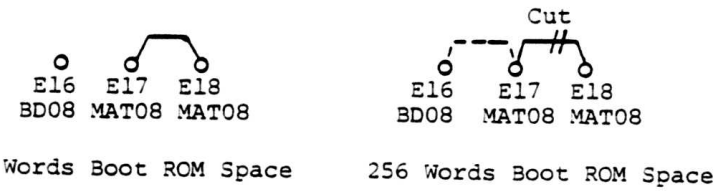


Boot PROM Address	7			7			3			0			0			0		
Address Line Number	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Boot PROM Address/Binary	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0
[1] Boot PROM Switch Settings [2]	X	X	X	X	X	O	C	O	O	C	X	X	X	X	X	X	X	X

1 O = Open or 1
C = Closed or 0
X = Do not Care

2 On boards shipped to SRI, the switches have been removed and wire wrap stakes put in their place. A closed switch position would then be equal to a wire wrap wire and an open switch position equal to no wire.

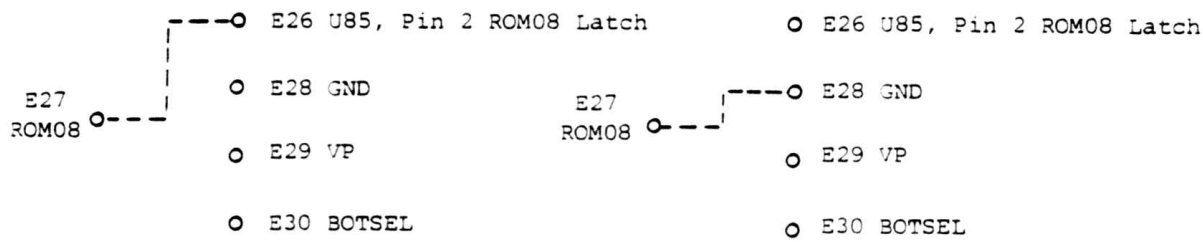
Figure 4-9



128 Words Boot ROM Space

256 Words Boot ROM Space

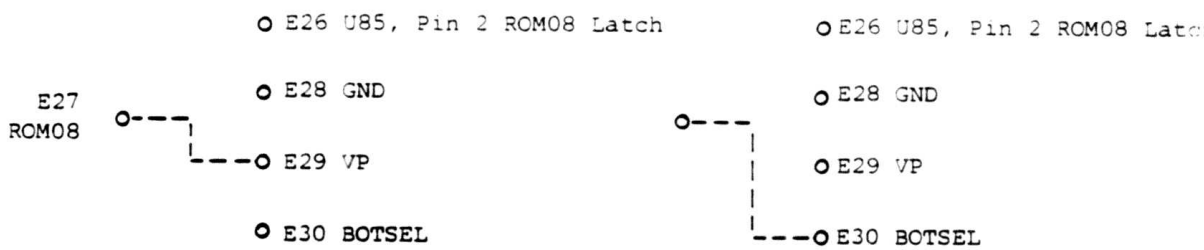
Figure 4-10



Address Controlled by Address Bus

Address Line Grounded, Selects First One-Fourth of ROM

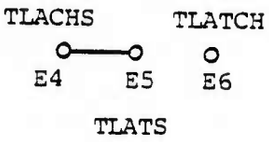
Figure 4-11



Address Line Pulled High (Up), Selects Second One-Fourth of ROM

Address Line Selected by Control Status Register Bit 6

Figure 4-12



Production Use Only

Figure 4-13

O E31 WRDOUT

Signal Deleted but Avaliable for Use

J2 layer 6, pins 26, 27, 28, and 29 are not attached directly to the ground plane, but are available for use when trace is cut. Used as extra signal lines on external bus.

Figure 4-14

CHAPTER 5

5.0 DRAWINGS, PARTS LIST, AND SCHEMATICS

Drawing Number	Revision Level	Date	Drawing Title
8100133 (4 sheets)	2	--	P.C. Assembly Robustness II Module
2600466 (6 sheets)	6	--	Logic Diagram Robustness II Module

ITEM NO.	QTY PER	FIG OR REF.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
44	1		6800098	PC BOARD ROBUSTNESS II
43	70		0000246	PWR AND GND CLIPS
42	110		0600011	WIRE WRAP STAKES
41	1		5400000	DEC PRGRM TRANS INTFC DCK11
40	2		0500014	SWITCH DIP 8 POS [illegible]
39	1		0300080	SOCKET 8 PIN DIP DIL808P108
38	2		0300053	CONNECTOR 40PIN RT ANGLE
37	1		0700176	CAP CER 2700pf
36	1		0700175	CAP CER .0022 mf
35	1		0700179	CAP CER .47uf

PARTS LIST

ITEM NO.	QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION
44	1		6800098	PC BOARD ROBUSTNESS II	
43	70		0000246	PWR AND GND CLIPS	
42	110		0600011	WIRE WRAP STAKES	
41	1		5400000	DEC PRGRM TRANSINTFC DCK11-AA	U1,2,4,5,11
40	2		0500014	SWITCH DIP 8POS 16KSB08S	U3, 71
39	1		0300080	SOCKET 8 PIN DIP DILB08P108	
38	2		0300053	CONNECTOR 40PIN RT ANGLE	J1, 2
37	1		0700176	CAP CER 2700pf	C6
36	1		0700175	CAP CER .0022 mf	C11
35	1		0700174	CAP CER .47uf	C10
34	2		0700103	CAP TAN	
33	10		0700099	CAP CER	
32	1		0700098	CAP CER	
31	1		0700075	RESISTO	
30	1		0700074	RESISTO	
29	9		0700071	RESISTO	
28	1		0700043	RESISTO	
27	1		0700032	RESIST	
26	1		0700029	RESISTO	
25	1		0500034	SWITCH R	
24	1		0400061	CRYSTAL	
23	2		0400050	DIP 15	
22	2		0300078	SOCKET	
21	28		0300075	SOCKET	
20	4		0300073	SOCKET	
19	26		0300072	SOCKET	
18	1		0100241	8-BIT DE	
17	1		0100269	DIVIDE E	
16	2		0100234	PROM 3	
15	2		0100216	QUAD IN	
14	1		0100182	8-BIT E	
13	5		0100169	DUAL 4	
12	5		0100164	OCTAL	
11	2		0100157	OCTAL	
10	12		0100150	OCT BUFF	
9	1		0100141	HEX D F	
8	3		0100117	DUAL D	
7	4		0100112	QUAD	
6	1		0100111	8-IN N	
5	1		0100110	TRIPLE	
4	2		0100103	QUAD 2	
3	4		0100102	HEX INV	
2	1		0100100	QUAD 2	
1	3		0100098	QUAD 2-I	

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS

DRAWN Wreddell

CHECKED M LOPER

ISSUED

DWG NO.	REV	SHT
8100133	2	1

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	2	PRELIMINARY	11/19/82	

ITEM NO.	QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION
34	2		0700103	CAP TANT RAD 6.8uF 35V 20%	C1, 2
33	10		0700099	CAP CER RAD .1uF 50V GEN PUR	C3, 7,8,9, C12 thru 17
32	1		0700098	CAP CER RAD .01uF 100V GEN PUR	C4
31	1		0700075	RESISTOR 6.8K OHM 1/8W 5%	R5
30	1		0700074	RESISTOR 4.7K OHM 1/8W 5%	R13
29	9		0700071	RESISTOR 1K OHM 1/8W 5%	R3,4,7,8,9,10,11,12,14
28	1		0700043	RESISTOR 10K OHM 1/4W 5%	R1
27	1		0700032	RESISTOR 1K OHM 1/4W 5%	R6
26	1		0700029	RESISTOR 680 OHM 1/4W 5%	R2
25	1		0500034	SWITCH RT ANGLE PC MOUNT TOGGLE	SW1
24	1		0400061	CRYSTAL OSC 1MHZ	Y1
23	2		0400050	DIP, 15 RES 16-PIN 47K OHM 2%	U70, 109
22	2		0300078	SOCKET 28-PIN DIP DILB28P-108	
21	28		0300075	SOCKET 20-PIN DIP DILB20P-108	
20	4		0300073	SOCKET 16-PIN DIP DILB16P-108	
19	26		0300072	SOCKET 14-PIN DIP DILB14P-108	
18	1		0100291	8-BIT DECODER W/CONT STOR 25LS2536	U150
17	1		0100269	DIVIDE BY 100 PRESCALER DS8629	U6
16	2		0100234	PROM 3-STATE OUTPUTS TBP28S42	U105, 106
15	2		0100216	QUAD UNIFIED BUS XCVR DS8641N	U9, 10
14	1		0100182	8-BIT EQUAL TO COMPARATOR LS521	U51
13	5		0100169	DUAL 4-BIT BI COUNT 74LS393	U21, 23, 42, 44, 66
12	5		0100164	OCTAL D F-F 74LS374	U22, 24, 41, 43, 85
11	2		0100157	OCTAL D F-F 74LS273	U87, 89
10	12		0100150	OCT BUFF DRVR NON INV 74LS244	91, U121 thru 124 UB1 thru B4, B6, B8, 90,
9	1		0100141	HEX D F-F SING RAIL OUT 74LS174	U6,9
8	3		0100117	DUAL D EDGE TRIG F-F 74LS74	U25, 31, 108
7	4		0100112	QUAD 2-IN OR GATE 74LS32	U29, 48, 61, 67
6	1		0100111	8-IN NAND GATE 74LS30	U63
5	1		0100110	TRIPLE 3-IN NOR GATE 74LS27	U107
4	2		0100103	QUAD 2-IN AND GATE 74LS08	U65, 68
3	4		0100102	HEX INVERTER 74LS04	U8, 30, 64, 110
2	1		0100100	QUAD 2-IN NOR GATE 74LS02	U49
1	3		0100098	QUAD 2-IN NAND GATE 74LS00	U45, 62, 111

PARTS LIST

ITEM NO.	QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION
				ROBUSTNESS II	
				END CLIPS	
				STAKES	
				TRANS INTFC DCKII-AA	U1,2,4,5,11
				8 POS 74LS8085	U3, 71
				N DIP DILB08P108	
				10PIN RT ANGLE	J1, 2
				0f	C6
				nf	C11
					C10

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

CONTRACT NO.

APPROVALS	DATE
DRAWN D Weddell	8NOV82
CHECKED M LOPER	11/9/82
ENGR	

MATERIAL

FINISH

DO NOT SCALE DRAWING

NEXT ASSY | USED ON

APPLICATION

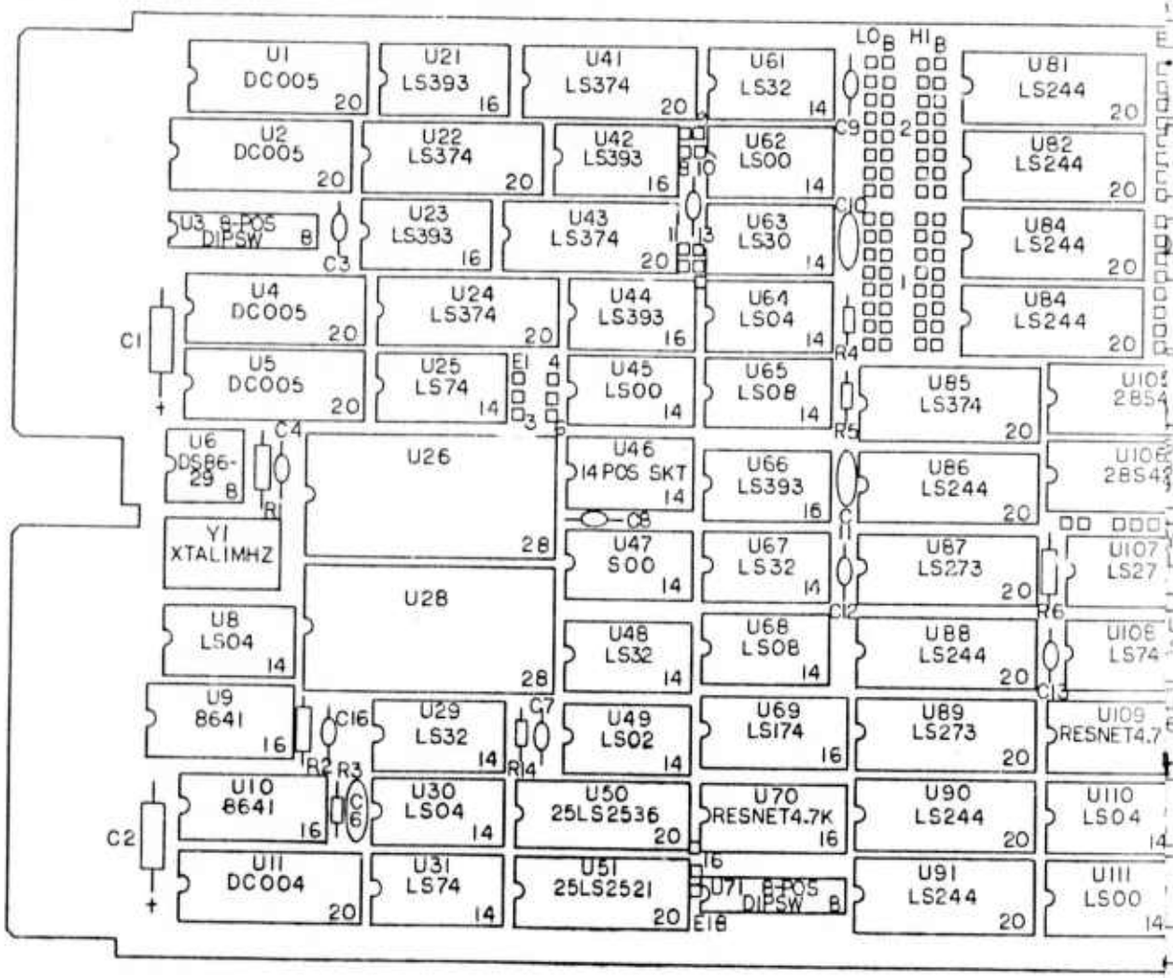
(A)

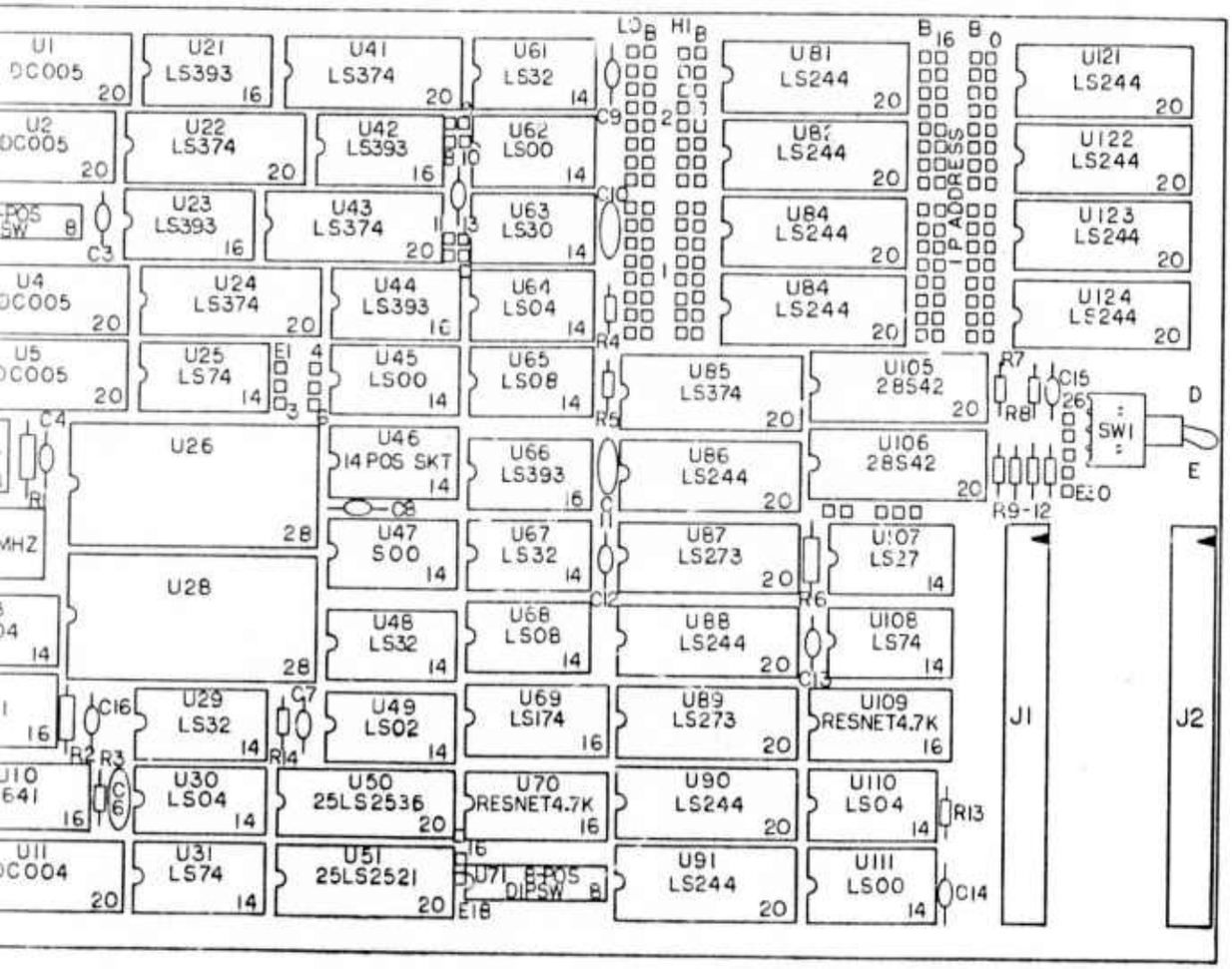
ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

PC ASSY
ROBUSTNESS II

SIZE	FSCM NO.	DWG NO.	REV
D	61550	8100133	2

SCALE NONE | SHEET 1 OF 4





ITEM NO.	QTY REQD	FSCM NO	PART OR IDENTIFYING NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS

MATERIAL

DRAWN Middell 29

CHECKED M LOPER 12

FINISH

ISSUED

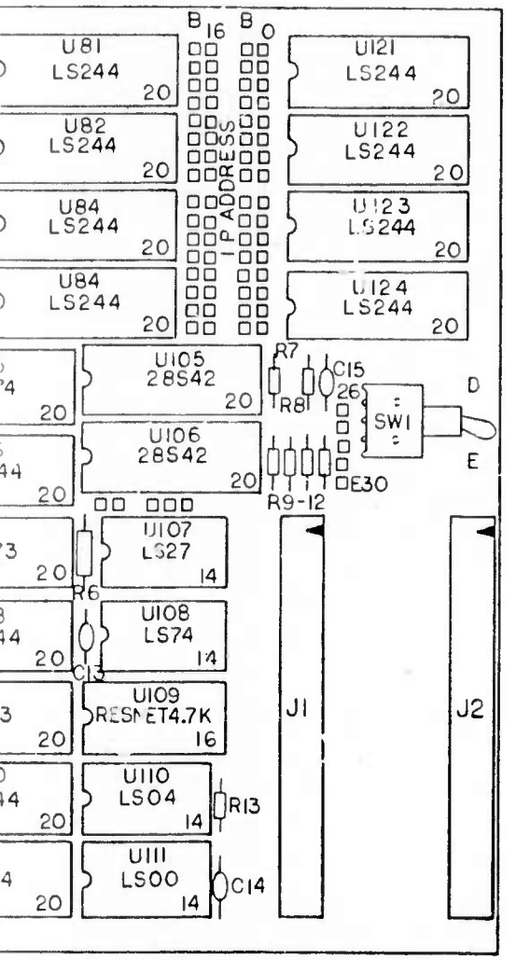
NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		



PC ASSEMBLY

ITEM NO.	QTY REQD	FSCM NO	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN Meddell	29NOV82
CHECKED M LOPER	12/1/82
ISSUED	

(A)

ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

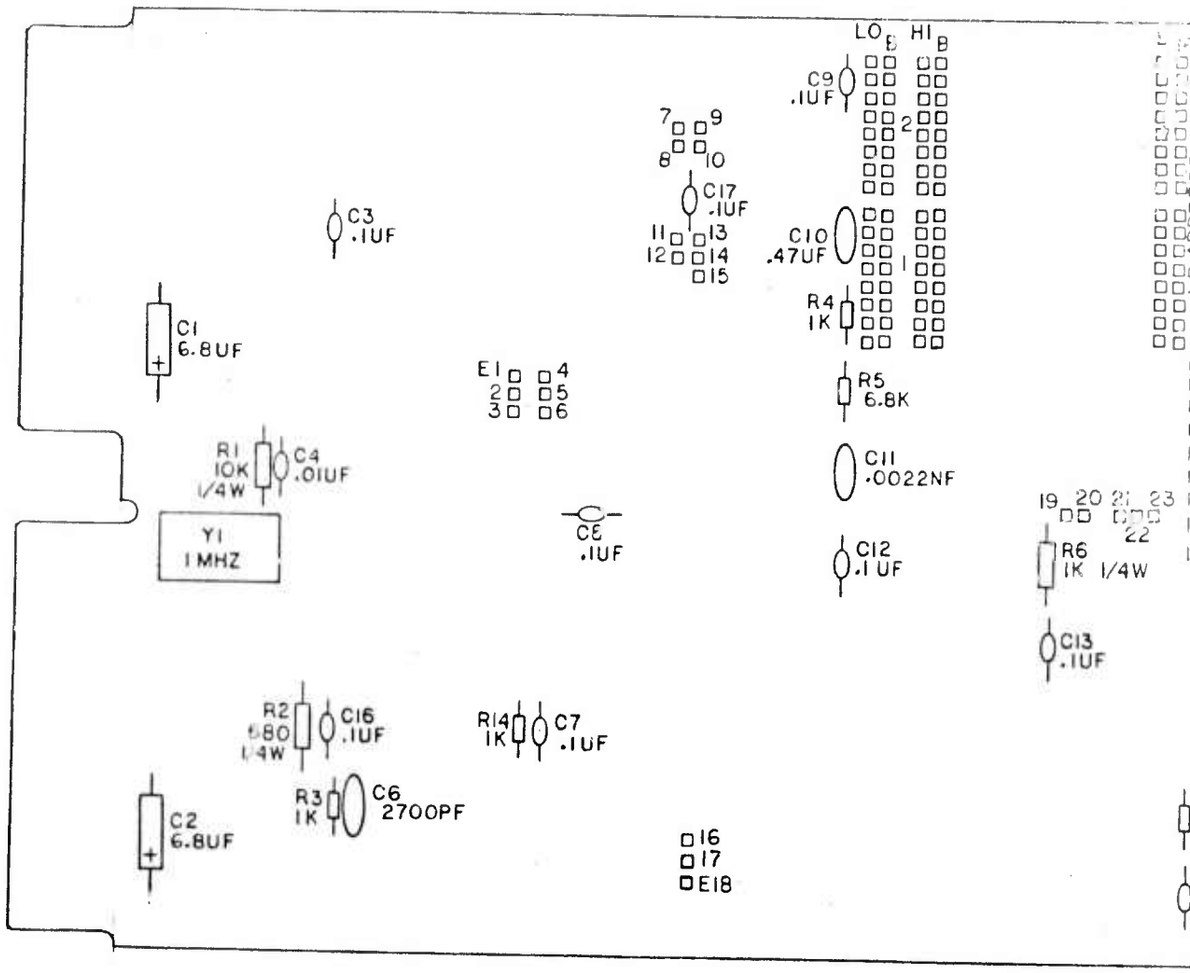
PC ASSY ROBUSTNESS II

SIZE	FSCM NO.	DWG. NO.	REV
D	61550	8100133	2

SCALE NONE SHEET 2 OF 4

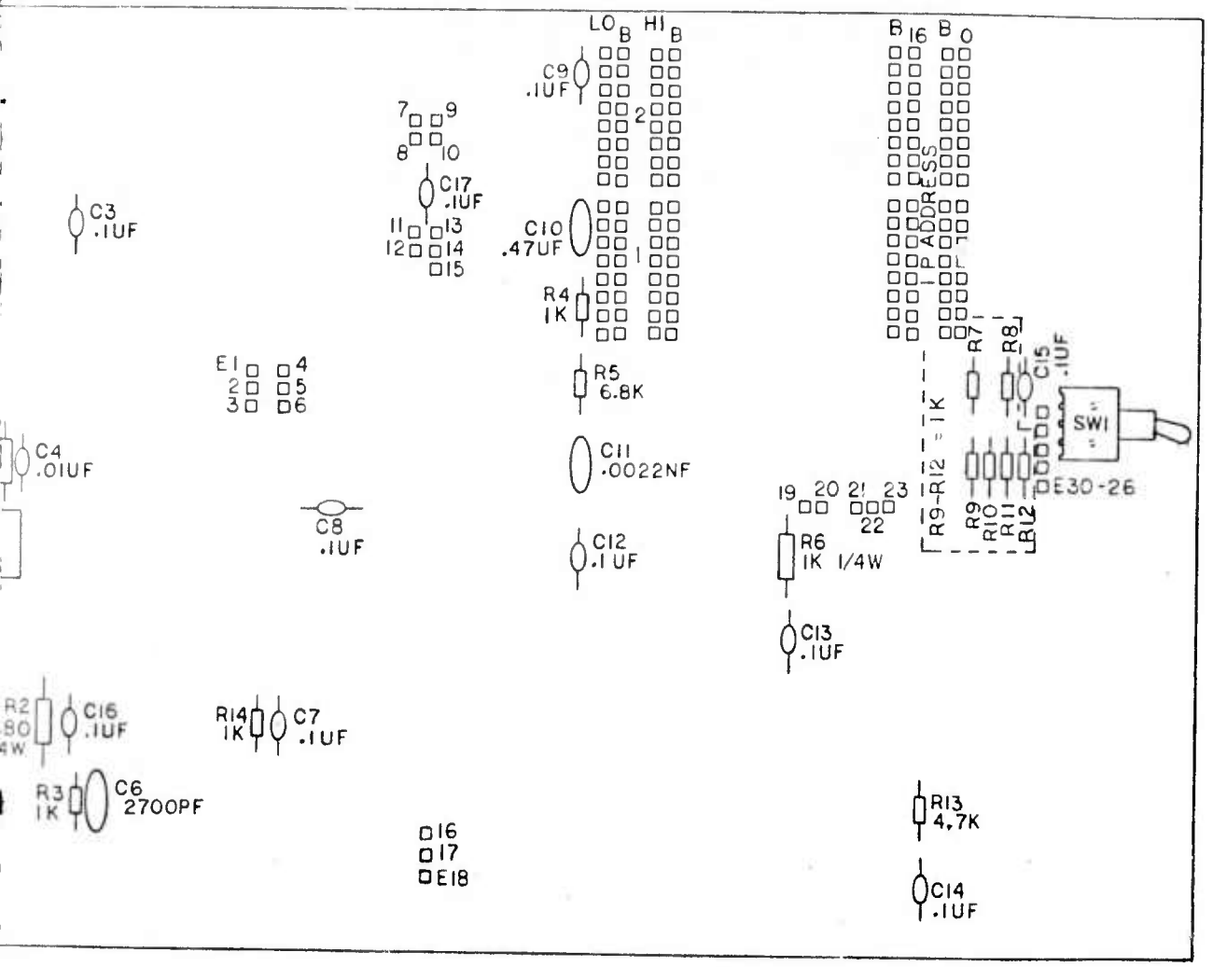
NEXT ASSY	USED ON
APPLICATION	

8100133 SH 2 REV 2



DWG NO 81

ZONE REV



W/W POS

ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS

MATERIAL

DRAWN MLOPER

CHECKED MLOPER

FINISH

ISSUED

NEXT ASSY | USED ON

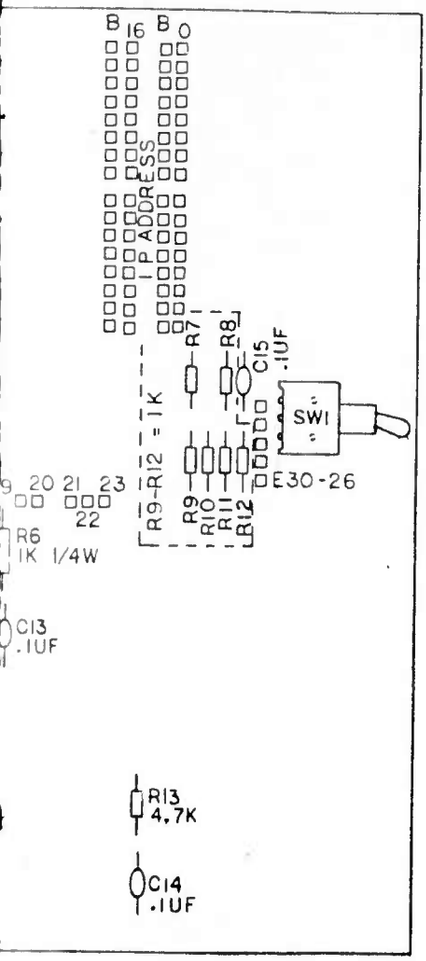
APPLICATION

DO NOT SCALE DRAWING

DWG NO	SH	REV
8100133	3	2

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SH1		



DWG NO	SH	REV
8100133	3	2

FAB GUIDE

W/W POSTS-DISCRETES-XTAL-SWITCH

ITEM NO	QTY REQD	PSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± .XXX ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN M Lopez	11/19/82
CHECKED M Lopez	11/19/82
ISSUED	

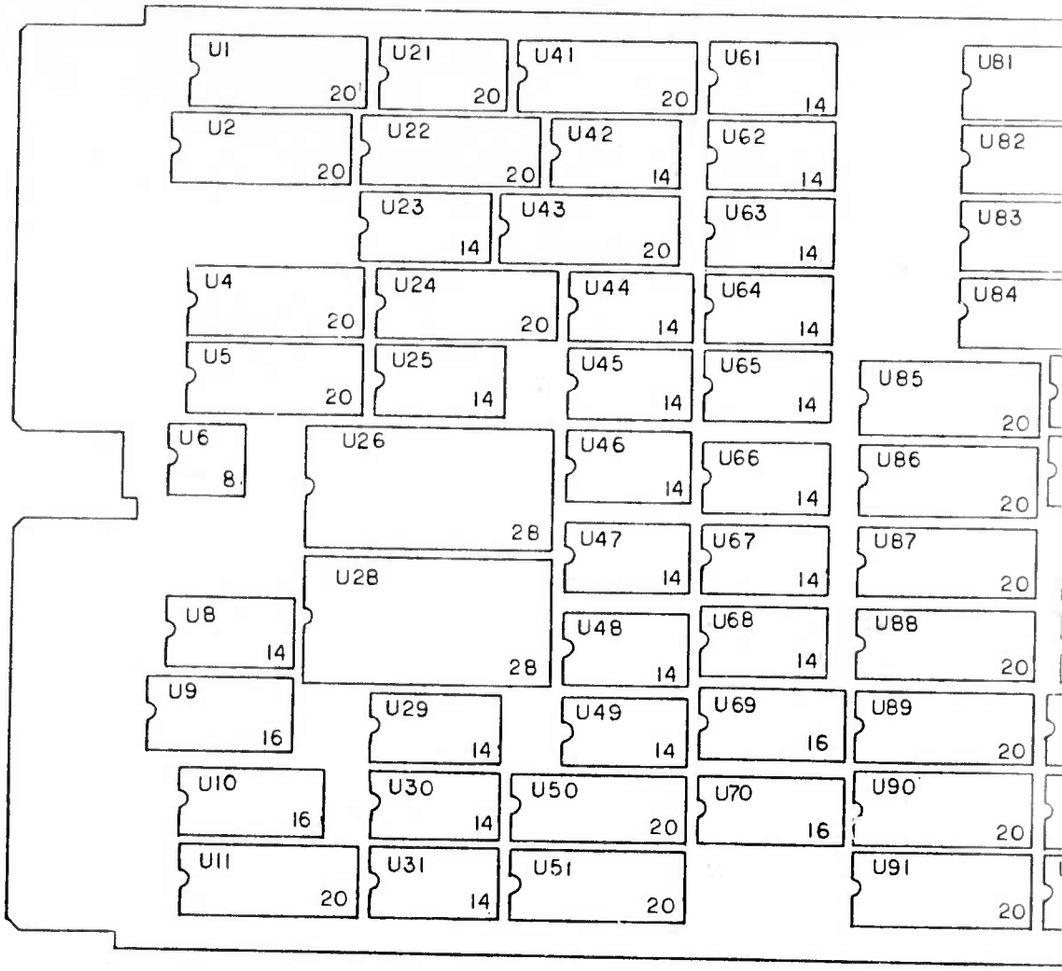
(A)

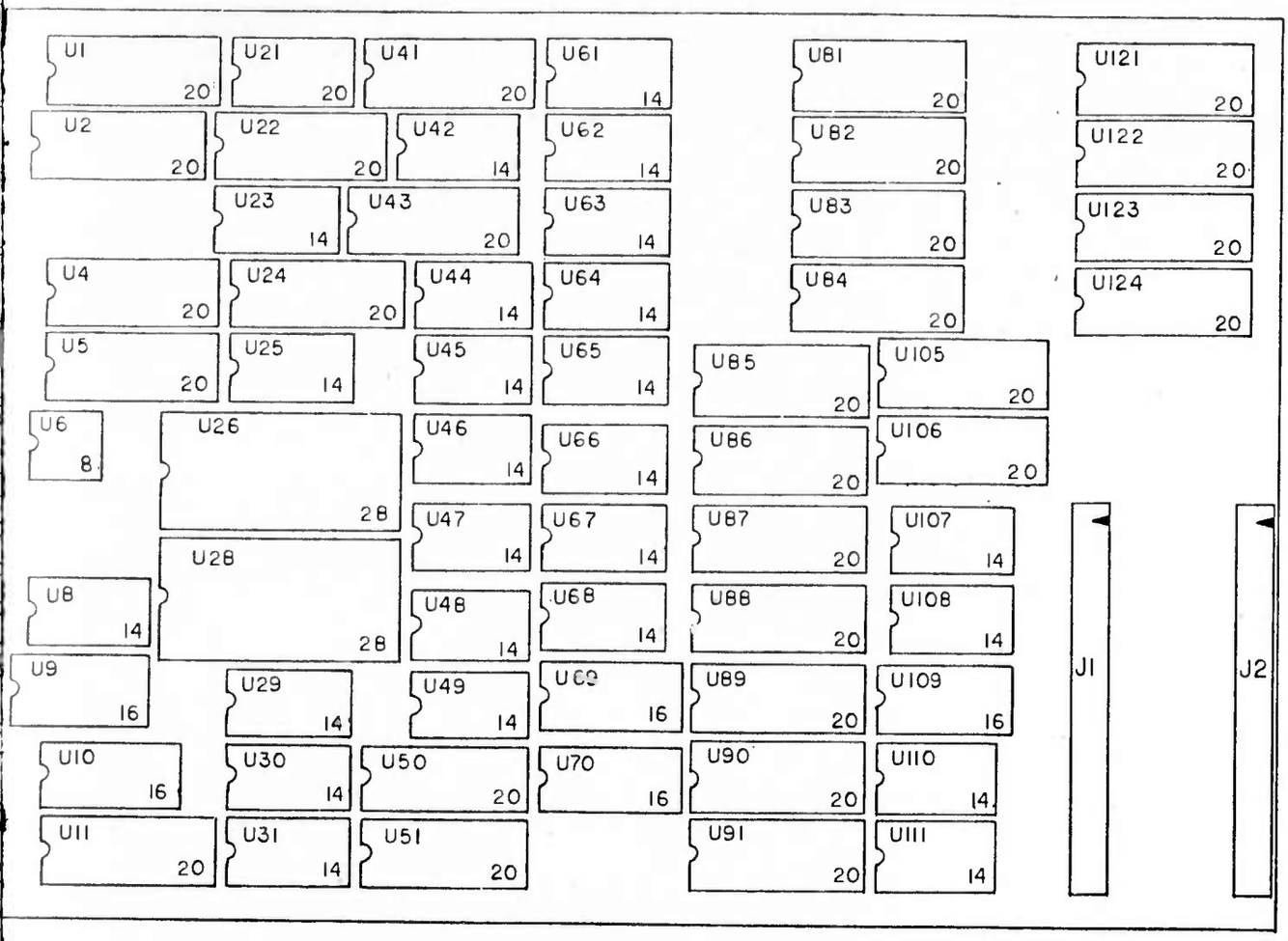
ACC ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

PC ASSY ROBUSTNESS II

SIZE	PSCM NO.	DWG. NO.	REV.
D	61550	8100133	2

SCALE 2:1 SHEET 3 OF 4





SO

ITEM NO.	QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

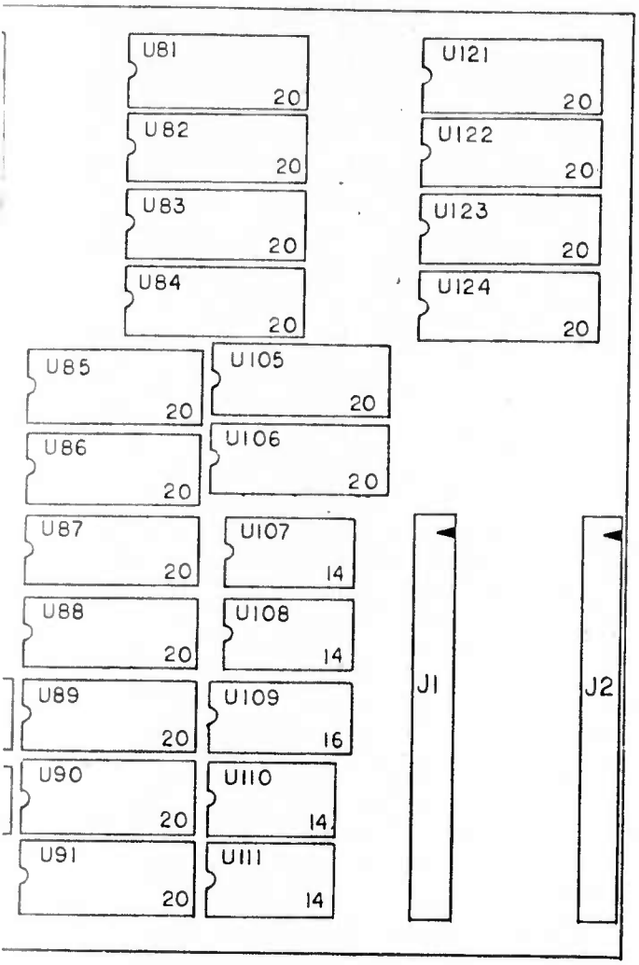
APPROVALS	DA
DRAWN Triddell	2/20
CHECKED MLOPER	12/1
ISSUED	

A

DWG NO 8100133 SH 4 REV 2

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		



FAB GUIDE
SOCKETS-CONNECTORS

PARTS LIST

ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES °

CONTRACT NO

ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

APPROVALS	DATE
DRAWN J Riddell	24NOV82
CHECKED M Loper	12/1/82
ISSUED	

MATERIAL

FINISH

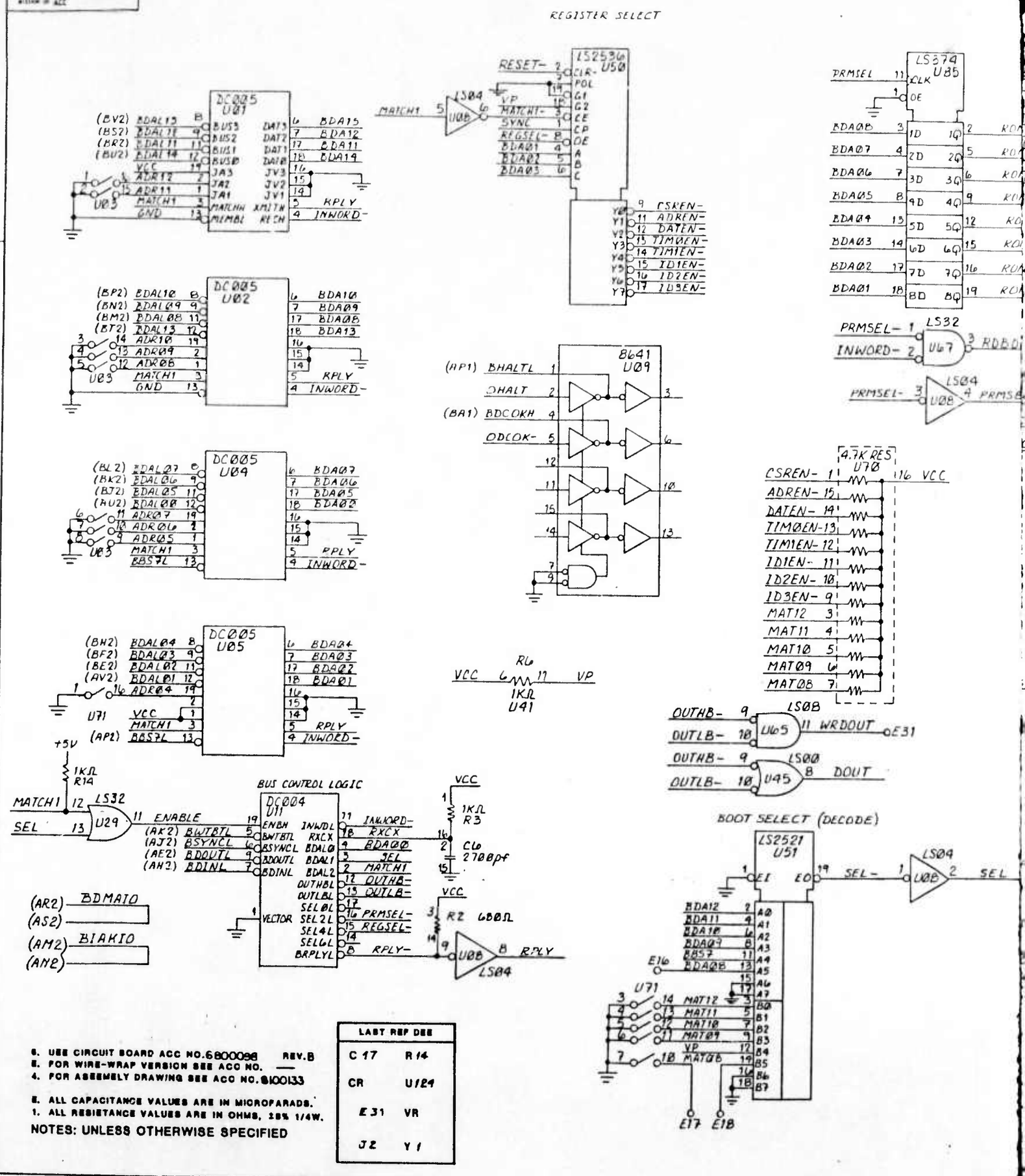
PC ASSY
ROBUSTNESS II

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

SIZE D | FSCM NO. 61550 | DWG. NO. 8100133 | REV. 2

SCALE 2/1 | SHEET 4 OF 4

(A)



LAST REF DES	
C 17	R 14
CR	U124
E 31	VR
J2	Y 1

6. USE CIRCUIT BOARD ACC NO.6800098 REV.B
5. FOR WIRE-WRAP VERSION SEE ACC NO. —
4. FOR ASSEMELY DRAWING SEE ACC NO. 8100133

3. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 25% 1/4W.

NOTES: UNLESS OTHERWISE SPECIFIED

DWG NO 2600466 REV

ZONE	REV	DESCRIPTION
	1	PRELIMINARY
	2	PRELIM.
	3	PRELIMINARY CHGD.
	4	PRELIM.
	5	PRELIM
	6	PRELIM

REGISTER SELECT

LS2536 U50
CLR- POL G1 G2 CE CP OE A B C
Y0 CSREN- Y1 ADREN- Y2 DATEN- Y3 TIMØEN- Y4 TIM1EN- Y5 ID1EN- Y6 ID2EN- Y7 ID3EN-

BOOT ROMS

LS374 U85
PRMSEL 11 CLK, 1 OE
BDAØB 3 1D 1Q 2 ROMØB
BDAØ7 4 2D 2Q 5 ROMØ7
BDAØ6 7 3D 3Q 6 ROMØ6
BDAØ5 8 4D 4Q 9 ROMØ5
BDAØ4 13 5D 5Q 12 ROMØ4
BDAØ3 14 6D 6Q 15 ROMØ3
BDAØ2 17 7D 7Q 16 ROMØ2
BDAØ1 18 8D 8Q 19 ROMØ1

BOTSEL E30
VP E29
E28
E26 E27

S472 U106
RDBOOT- 15 CE-
E20 E19
ROMØB 18 A7 D7 13 BDA14
ROMØ7 17 A6 D6 12 BDA13
ROMØ6 16 A5 D5 11 BDA12
ROMØ5 5 A4 D4 9 BDA11
ROMØ4 4 A3 D3 8 BDA1Ø
ROMØ3 3 A2 D2 7 BDAØ9
ROMØ2 2 A1 D1 6 BDAØ8
ROMØ1 1 AØ

PRMSEL- 1, INWORD- 2 → LS32 U67 → 3 RDBOOT-
PRMSEL- 3 → LSØ4 U8B → 4 PRMSEL

S472 U105
RDBOOT- 15 CE-
19 AB DB 14 BDAØ7
ROMØB 18 A7 D7 13 BDAØ6
ROMØ7 17 A6 D6 12 BDAØ5
ROMØ6 16 A5 D5 11 BDAØ4
ROMØ5 5 A4 D4 9 BDAØ3
ROMØ4 4 A3 D3 8 BDAØ2
ROMØ3 3 A2 D2 7 BDAØ1
ROMØ2 2 A1 D1 6 BDAØØ
ROMØ1 1 AØ

8641 U09
LTL 1, LT 2, OKH 4, OK- 5, 12, 11, 15, 14, 7, 9 → 3, 6, 10, 13

4.7K RES U70
CSREN- 1 … 16 VCC
ADREN- 15
DATEN- 14
TIMØEN- 13
TIM1EN- 12
ID1EN- 11
ID2EN- 10
ID3EN- 9
MAT12 3
MAT11 4
MAT10 5
MAT09 6
MATØ8 7

RØ 17 VP
1KΩ
U41

OUTHB- 9, OUTLB- 10 → LSØ8 U65 → 11 WRDOUT → E31
OUTHB- 9, OUTLB- 10 → LSØØ U45 → 8 DOUT

BOOT SELECT (DECODE)

LS2521 U51
E1 E0 19 SEL- → LSØ4 U8B → 2 SEL
BDA12 2 A0
BDA11 4 A1
BDA10 6 A2
BDAØ9 8 A3
BBS7 11 A4
E16 BDAØB 13 A5
15 A6
17 A7
U71
3 14 MAT12 3 B0
4 13 MAT11 5 B1
5 12 MAT10 7 B2
6 11 MAT09 9 B3
VP 12 B4
7 10 MATØ8 19 B5
16 B6
18 B7
E17 E18

RPLY

8641 U10
(AP2) BBS7L 1 → 3 BBS7
(AJ2) BSYNCL 4 → 6 SYNC
(AF2) BRPLYL 12
RPLY 11 → 10
(AT2) BINITL 15
14 → 13 RESET 13
7, 9
LSØ4 U3Ø 12 RESET-

BUS INTERFACE, SELECTION LO

ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

CONTRACT NO

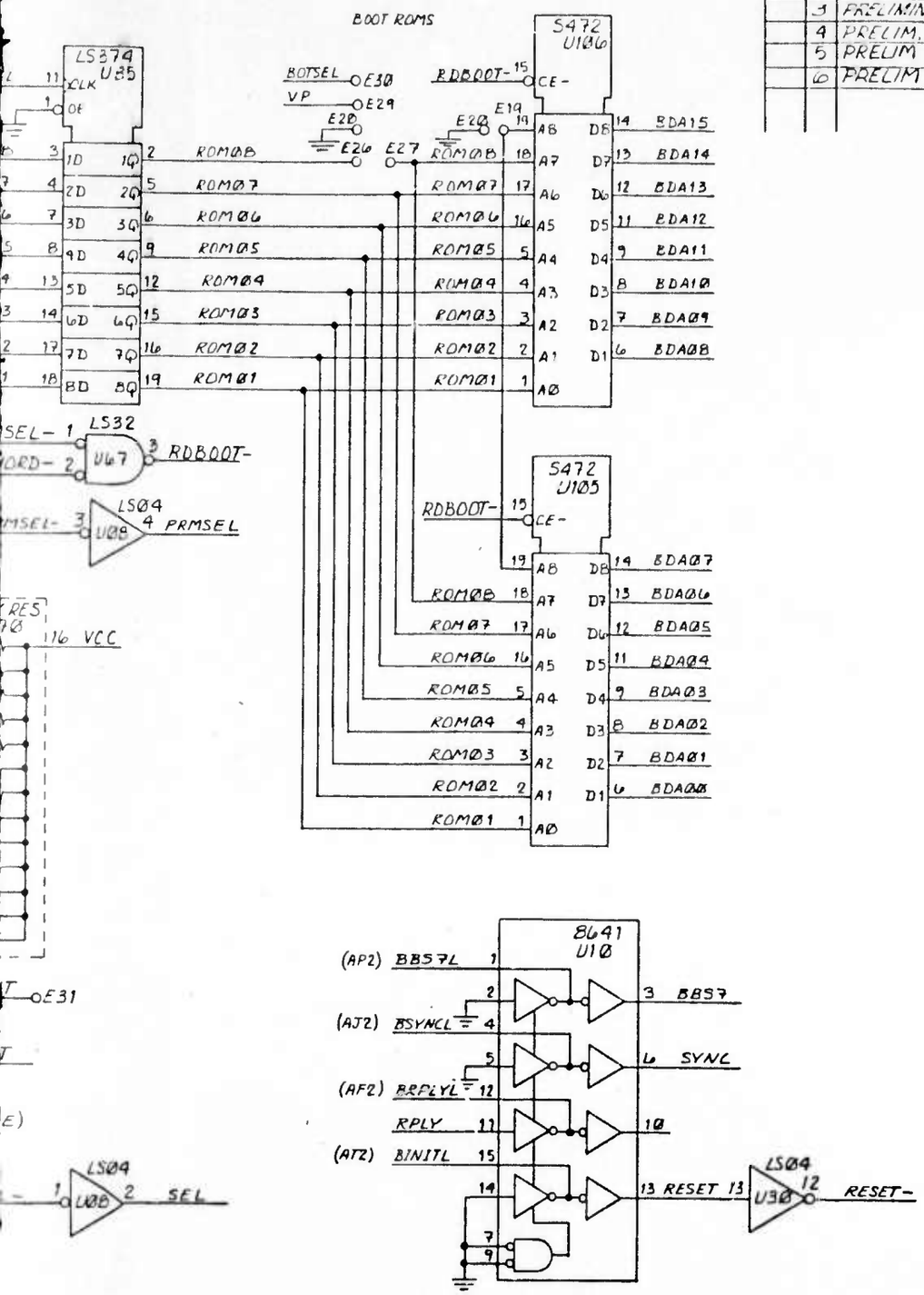
APPROVALS	DATE
DRAWN WEDDELL	2-4-82
CHECKED M. Lang	10/4/82
ISSUED	

MATERIAL
FINISH
NEXT ASSY USED ON
APPLICATION DO NOT SCALE DRAWING

ACC ASSY
LO
ROBU
SIZE D FSCM NO 61550
SCALE NONE

DWG NO 2600466 SH 1 REV 6

ZONE	REV	DESCRIPTION	DATE	APPROVED
	1	PRELIMINARY	2 FEB 82	
	2	PRELIM.	3 22 82	
	3	PRELIMINARY CHG'D. SHTS. 1	3-24-82	
	4	PRELIM.	9 APR 82	
	5	PRELIM	9 NOV 82	
	6	PRELIM	22 NOV 82	



BUS INTERFACE, SELECTION LOGIC, BOOT PROM

ITEM NO.	QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

CONTRACT NO

ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

APPROVALS	DATE
DRAWN WEDDELL	2-4-82
CHECKED M. Lowe	10/4/82
ISSUED	

MATERIAL
FINISH

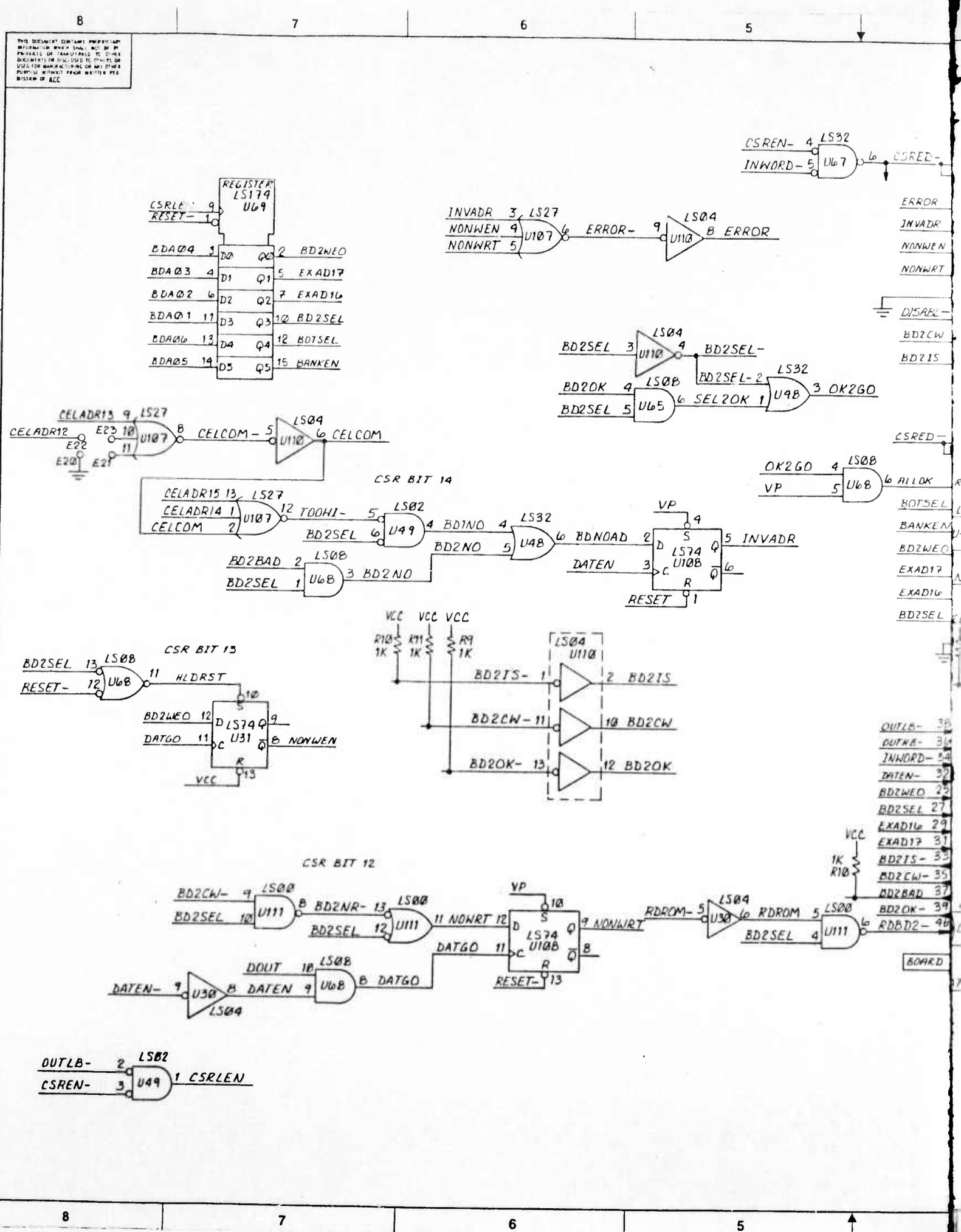
NEXT ASSY | USED ON
APPLICATION | DO NOT SCALE DRAWING

© ACC

LOGIC DIAGRAM
ROBUSTNESS II MOD

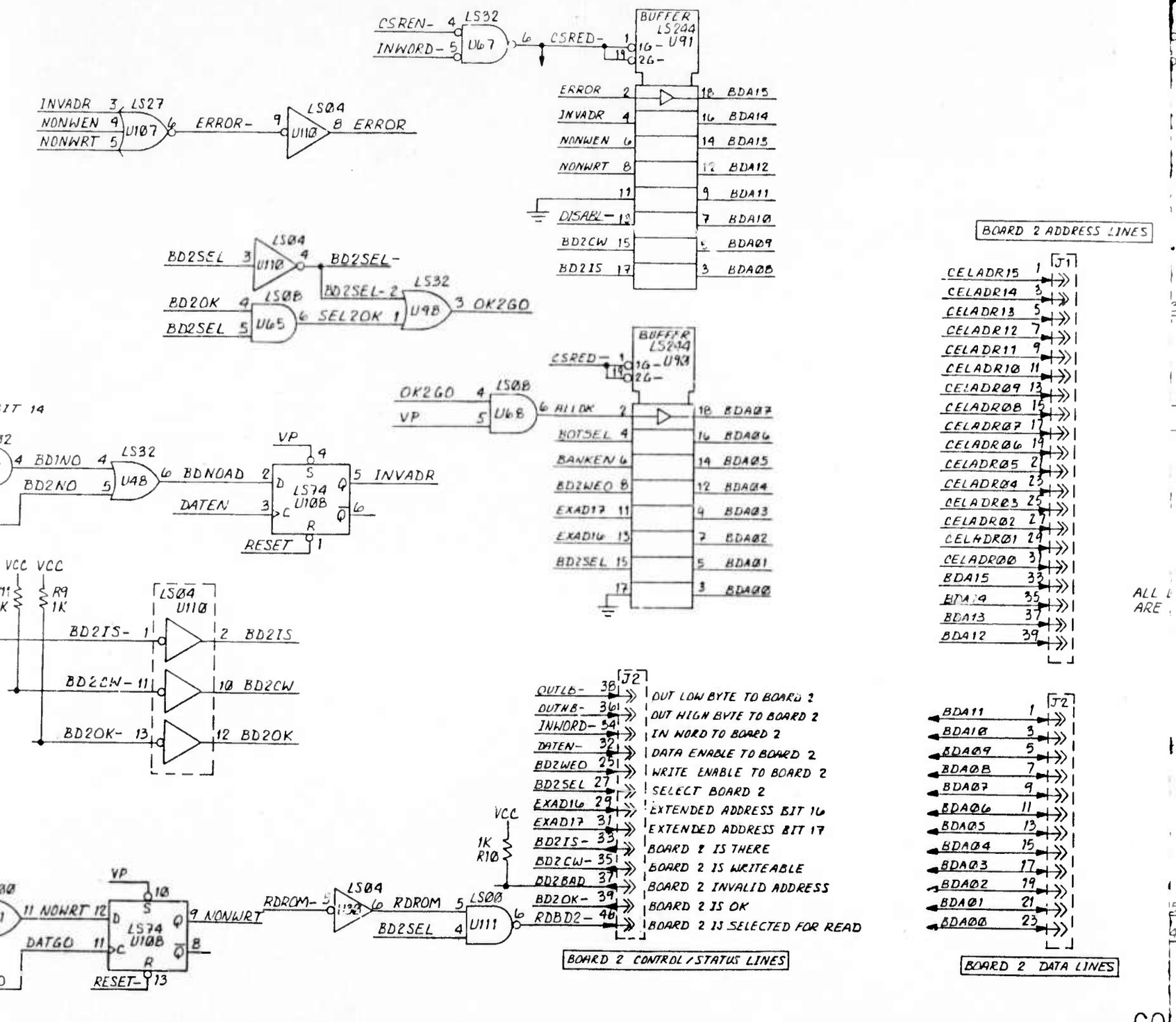
SIZE D | FSCM NO 61550 | DWG. NO. 2600466 | REV 6
SCALE NONE | SHEET 1 OF 6

DWG NO 2600466 SH 1 REV 6



DWG NO 2600

ZONE | REV | SEE



ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO

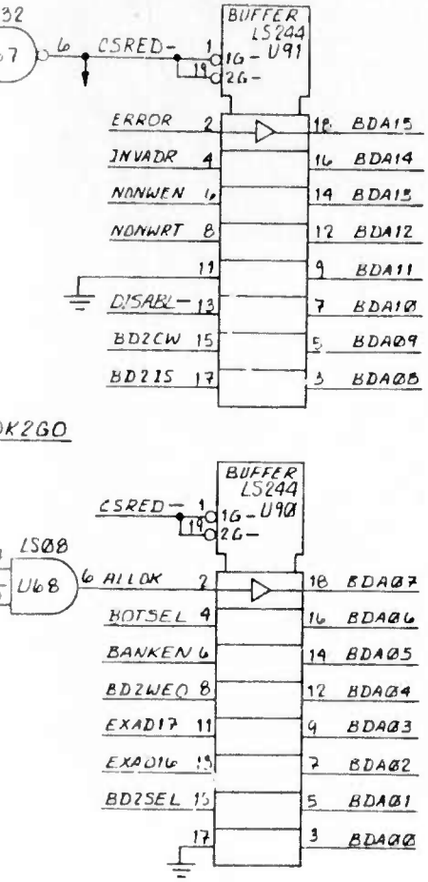
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

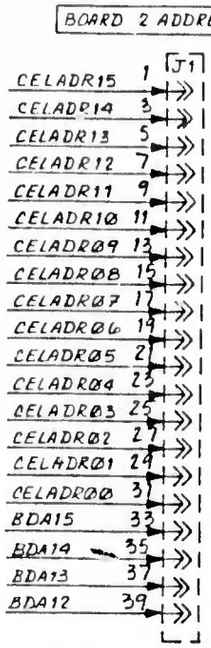
APPROVALS	DATE
DRAWN AJEDDELL	8-4-82
CHECKED [illegible]	10/4/82
ISSUED	

MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION | DO NOT SCALE DRAWING

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SH 1		





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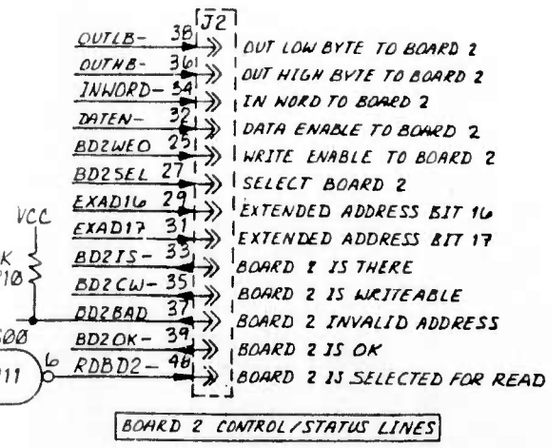
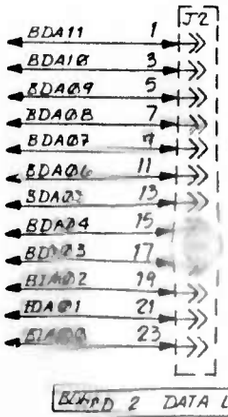




CONTROL STATUS REGISTER AND EXTERNAL BUS TO BD NO 2

PARTS LIST

ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

CONTRACT NO

ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

APPROVALS	DATE
DRAWN WEDDELL	8-9-82
CHECKED M Lopez	10/4/82
ISSUED	

LOGIC DIAGRAM
ROBUSTNESS II MOD

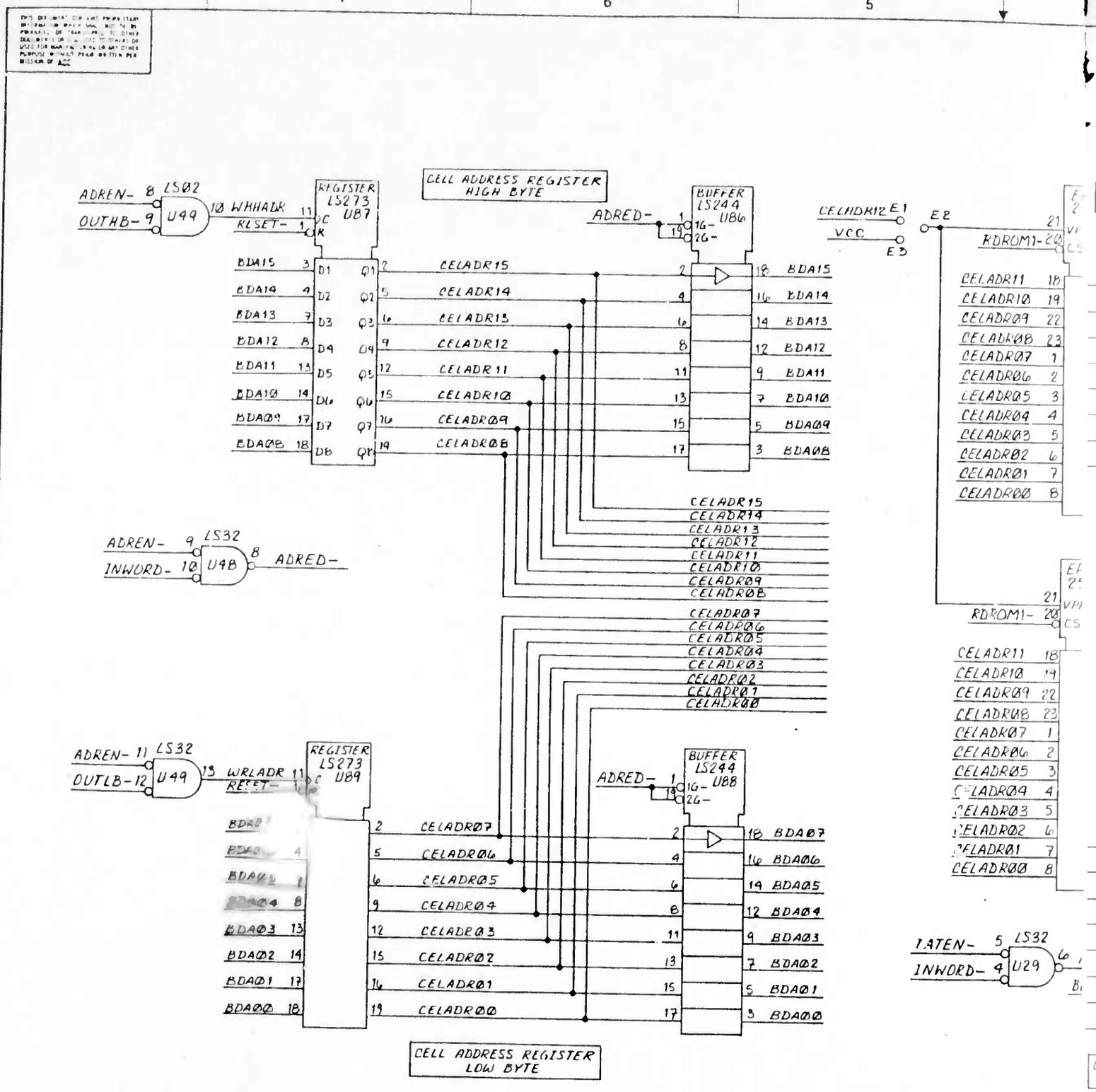
NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

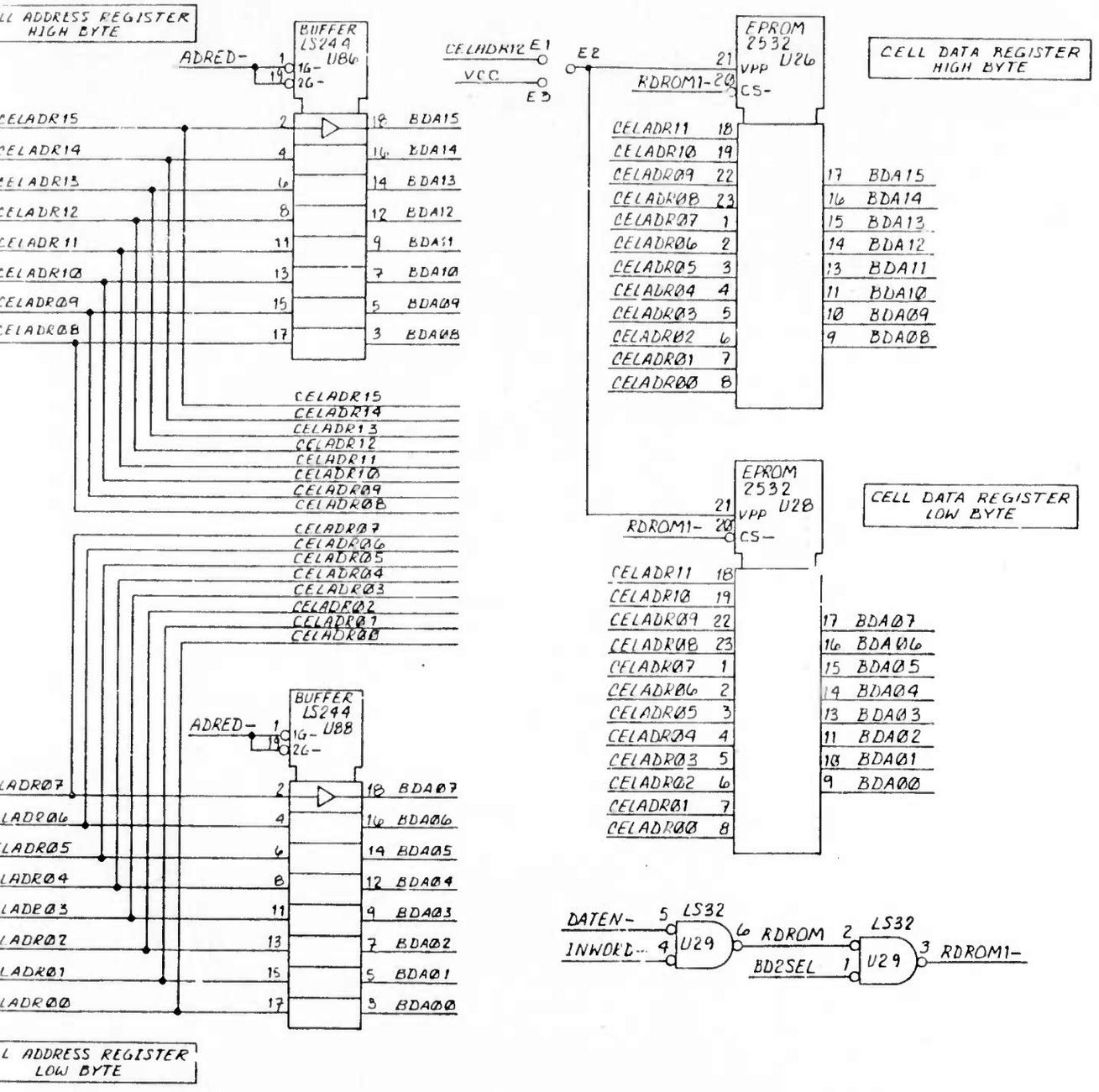
MATERIAL
FINISH

©

SIZE D | FSCM NO 61550 | DWG NO 2600466 | REV 6
SCALE NONE | SHEET 2 OF 6

2600466 SH 2 REV 6


CELL ADDRESS REGISTER HIGH BYTE
ADREN- 8 LS02 U49 10 WRHADR
OUTHB- 9
RESET- 1
REGISTER LS273 U87
BUFFER LS244 U86
ADRED- 1G- 2G-
BDA15 BDA14 BDA13 BDA12 BDA11 BDA10 BDA09 BDA08
CELADR15 CELADR14 CELADR13 CELADR12 CELADR11 CELADR10 CELADR09 CELADR08
CELADR15 CELADR14 CELADR13 CELADR12 CELADR11 CELADR10 CELADR09 CELADR08
CELADR07 CELADR06 CELADR05 CELADR04 CELADR03 CELADR02 CELADR01 CELADR00
ADREN- 9 LS32 U48 8 ADRED-
INWORD- 10
ADREN- 11 LS32 U49 13 WRLADR
OUTLB- 12
RESET-
REGISTER LS273 U89
BUFFER LS244 U88
ADRED- 1G- 2G-
BDA07 BDA06 BDA05 BDA04 BDA03 BDA02 BDA01 BDA00
CELADR07 CELADR06 CELADR05 CELADR04 CELADR03 CELADR02 CELADR01 CELADR00
CELADR12 E1
VCC E3
E2
RDROM1- 20
CELADR11 CELADR10 CELADR09 CELADR08 CELADR07 CELADR06 CELADR05 CELADR04 CELADR03 CELADR02 CELADR01 CELADR00
RDROM1- 20
CELADR11 CELADR10 CELADR09 CELADR08 CELADR07 CELADR06 CELADR05 CELADR04 CELADR03 CELADR02 CELADR01 CELADR00
LATEN- 5 LS32 U29 6
INWORD- 4
CELL ADDRESS REGISTER LOW BYTE



CELL AD

ITEM NO	QTY REQD	FROM NO.	PART OR IDENTIFYING NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.X ±
.XXX ±

CONTRACT NO

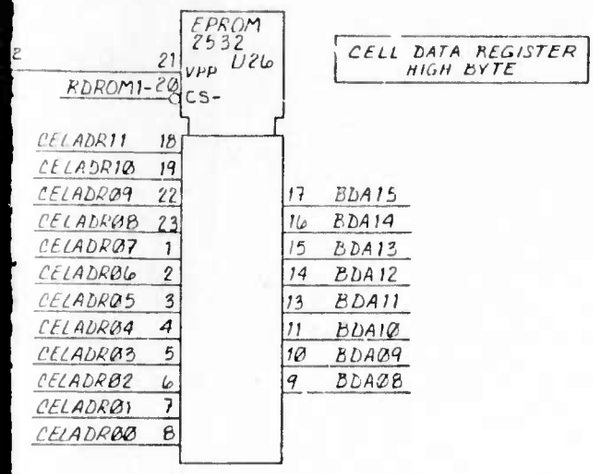
APPROVALS
DRAWN WEDDELL
CHECKED
ISSUED

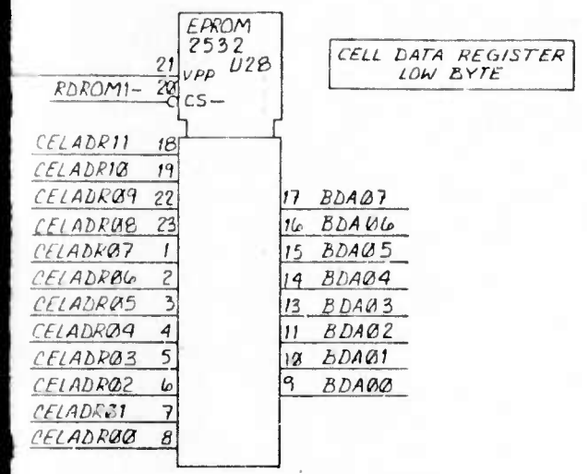
MATERIAL
FINISH

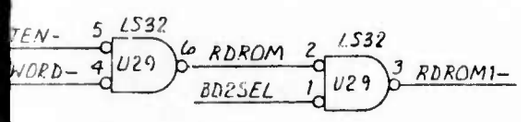
NEXT ASSY | USED ON
APPLICATION | DO NOT SCALE DRAWING

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SH 1		







CELL ADDRESS AND DATA REGISTERS

PARTS LIST

ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

CONTRACT NO

APPROVALS	DATE
DRAWN WEDDELL	2-4-82
CHECKED ML Lowe	2/4/82
ISSUED	

MATERIAL

FINISH

DO NOT SCALE DRAWING

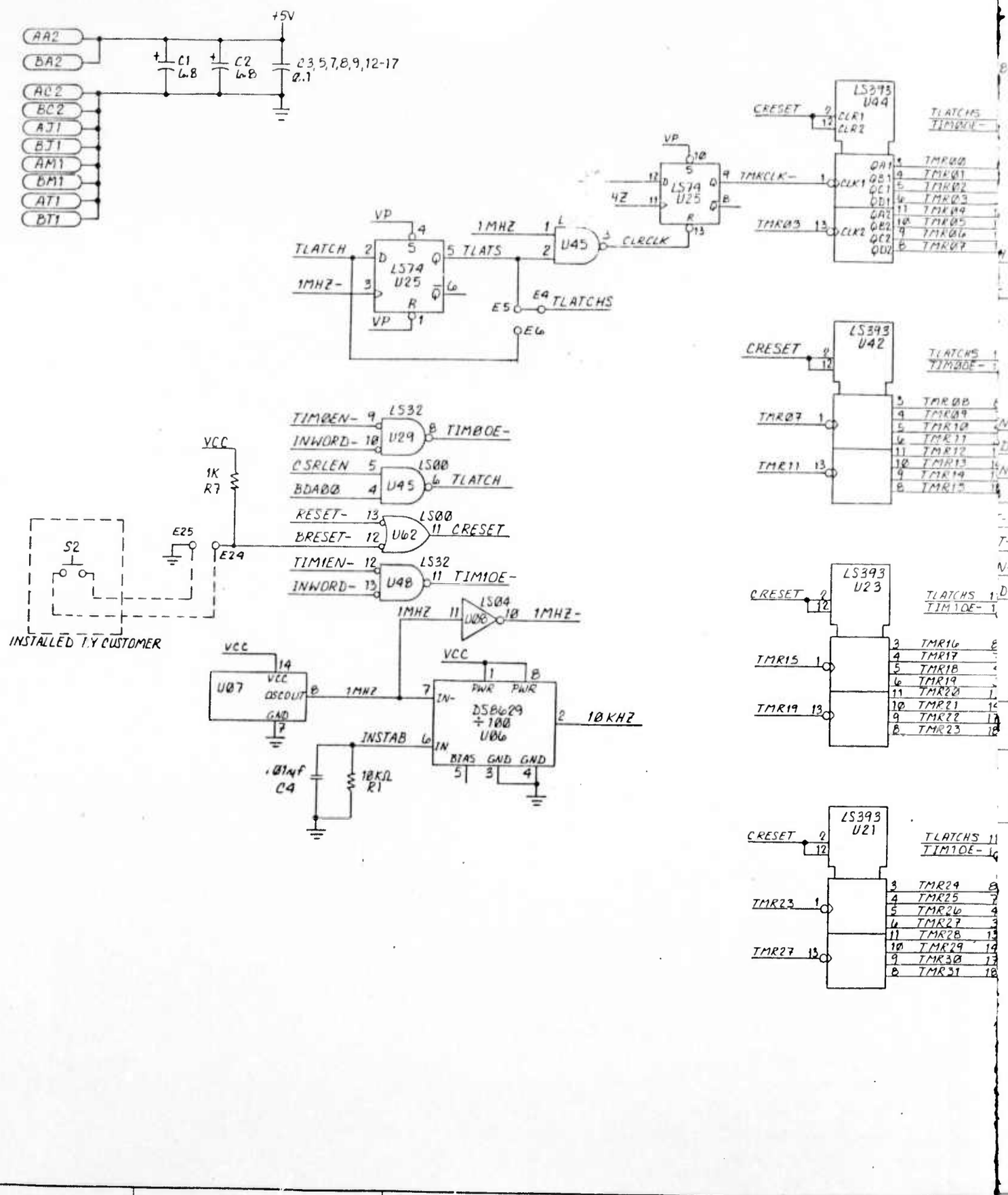
©

LOGIC DIAGRAM
ROBUSTNESS II MOD

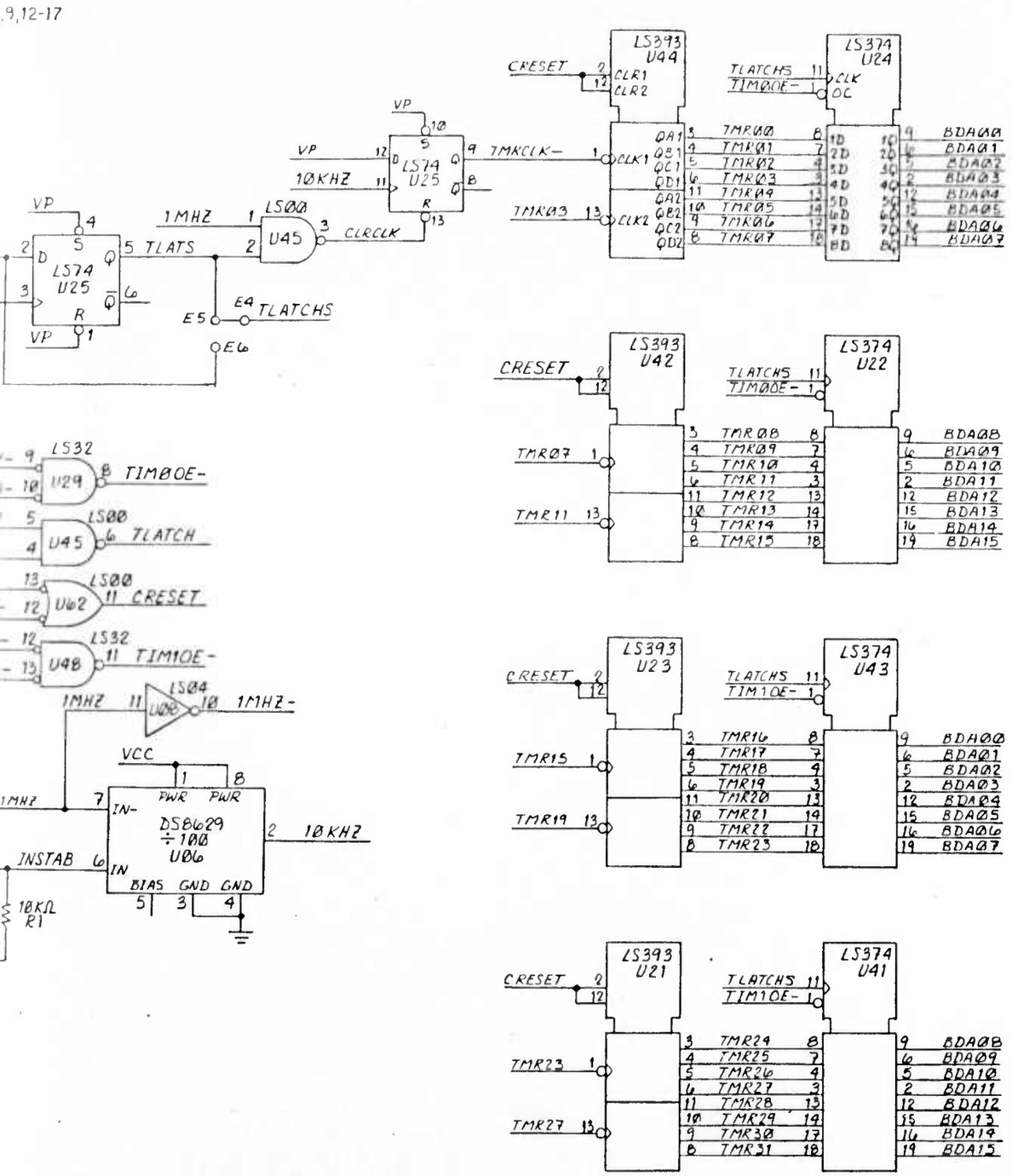
NEXT ASSY	USED ON
APPLICATION	

SIZE	FSCM NO.	DWG. NO.	REV
D	61550	2600466	6

SCALE NONE SHEET 3 OF 6


+5V
AA2
BA2
AC2
BC2
AJ1
BJ1
AM1
BM1
AT1
BT1
C1 6.8
C2 6.8
C3,5,7,8,9,12-17 0.1
VP
LS74 U25
TLATCH
1MHZ-
TLATS
1MHZ
U45
CLRCLK
E5
E4 TLATCHS
E6
LS393 U44
CRESET
TLATCHS
TIM0OE-
TMRCLK-
TMR03
TMR00
TMR01
TMR02
TMR03
TMR04
TMR05
TMR06
TMR07
LS393 U42
TMR07
TMR11
TMR08
TMR09
TMR10
TMR11
TMR12
TMR13
TMR14
TMR15
LS393 U23
TMR15
TMR19
TMR16
TMR17
TMR18
TMR19
TMR20
TMR21
TMR22
TMR23
LS393 U21
TMR23
TMR27
TMR24
TMR25
TMR26
TMR27
TMR28
TMR29
TMR30
TMR31
TIM0EN-
INWORD-
LS32 U29
TIM0OE-
CSRLEN
BDA00
LS00 U45
TLATCH
RESET-
BRESET-
LS00 U62
CRESET
TIM1EN-
INWORD-
LS32 U48
TIM1OE-
LS04 U08
1MHZ-
VCC
1K R7
E25
E24
S2
INSTALLED T.Y CUSTOMER
U07
OSCOUT
GND
INSTAB
.01uf C4
10KΩ R1
DS8629 ÷100 U06
PWR
IN-
IN
BIAS
10KHZ

,9,12-17



TIMER A

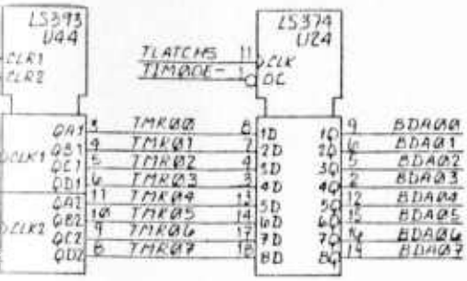
ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO

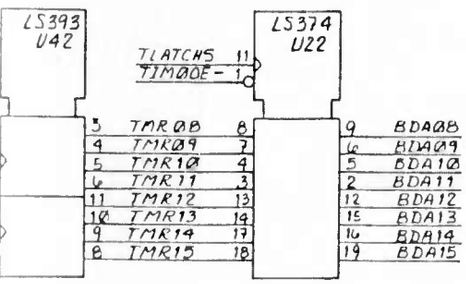
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.
APPROVALS
MATERIAL
DRAWN WEDDELL
CHECKED
FINISH
ISSUED
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING

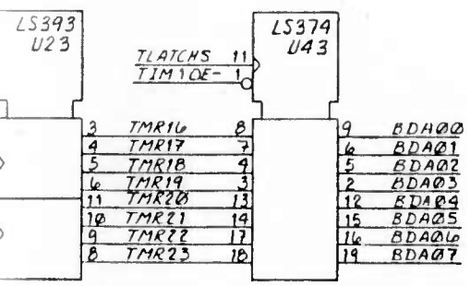
REVISIONS

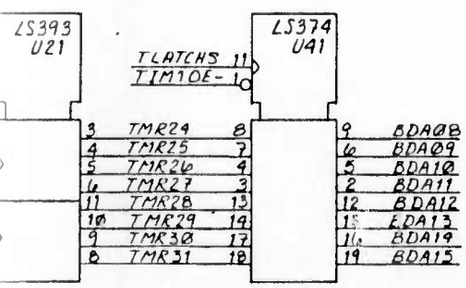
ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SH 1		





TMR04 — E11
TMR05 — E13
TMR06 — E12
TMR07 — E14
TMR08 — E7
TMR09 — E9
TMR10 — E8
TMR11 — E10





TIMER AND TIMER REGISTER 1 AND 2

ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN WEDDELL	2-4-82
CHECKED	11/4/82
ISSUED	

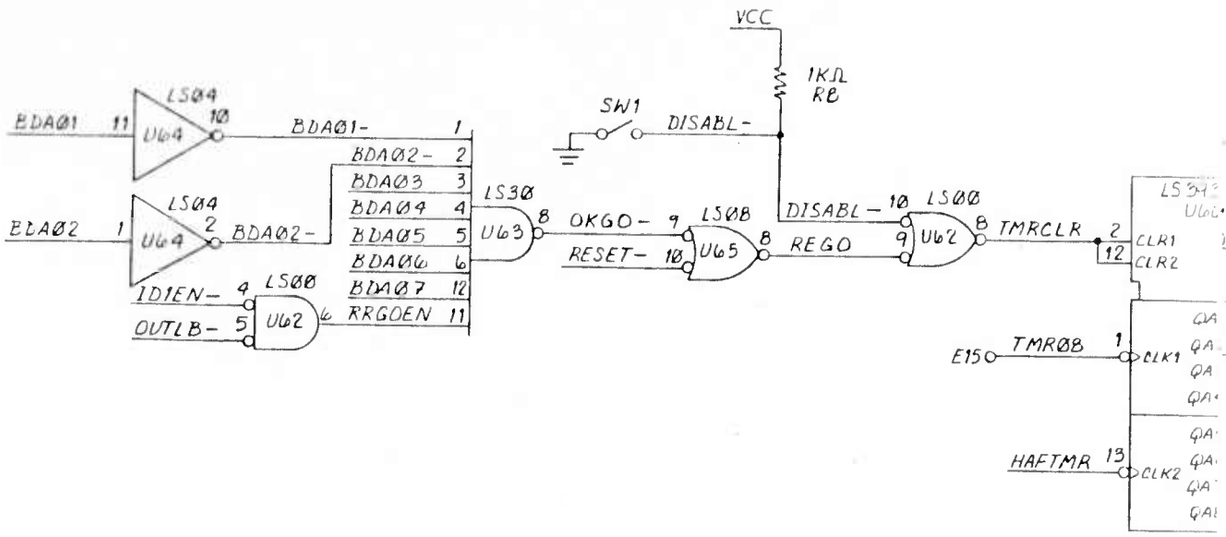
ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

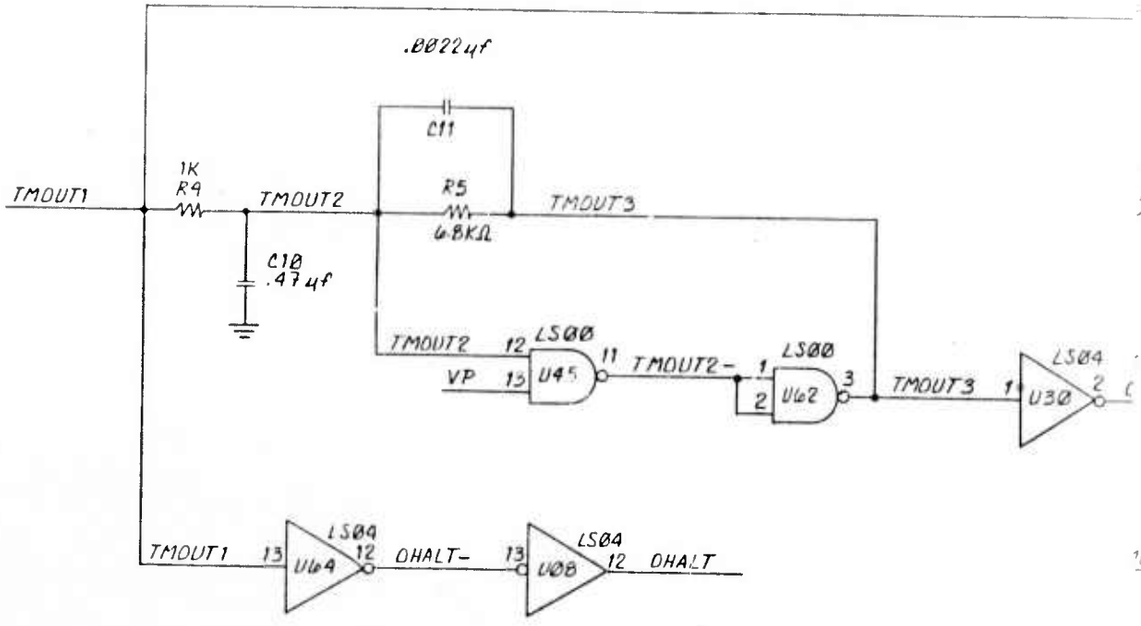
LOGIC DIAGRAM
ROBUSTNESS II MOD

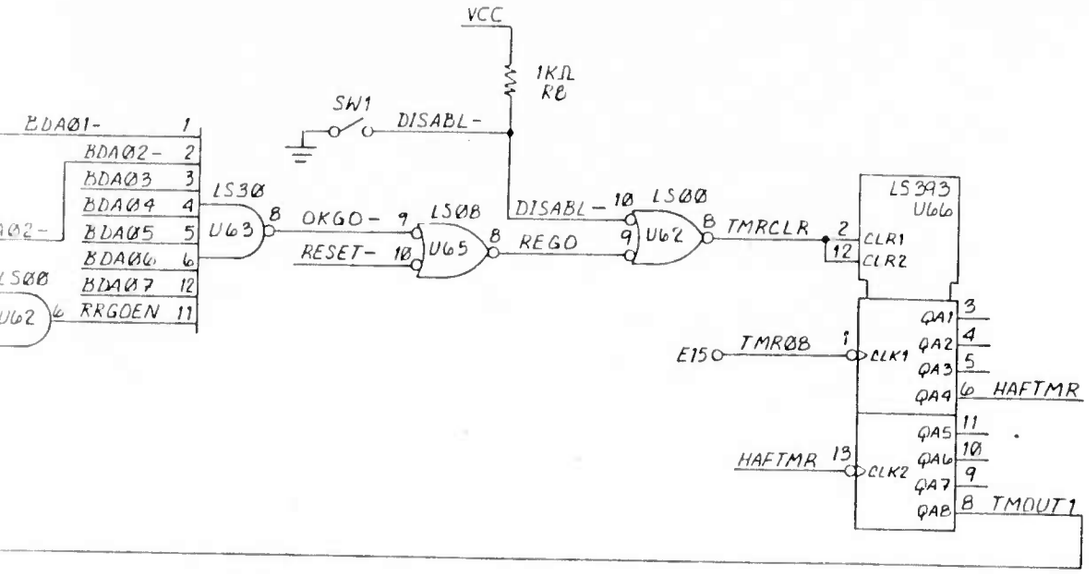
SIZE D | FSCM NO 61550 | DWG. NO. 2600466 | REV 6

SCALE NONE | SHEET 4 OF 6

DWG NO 2600466 SH 4 REV 6







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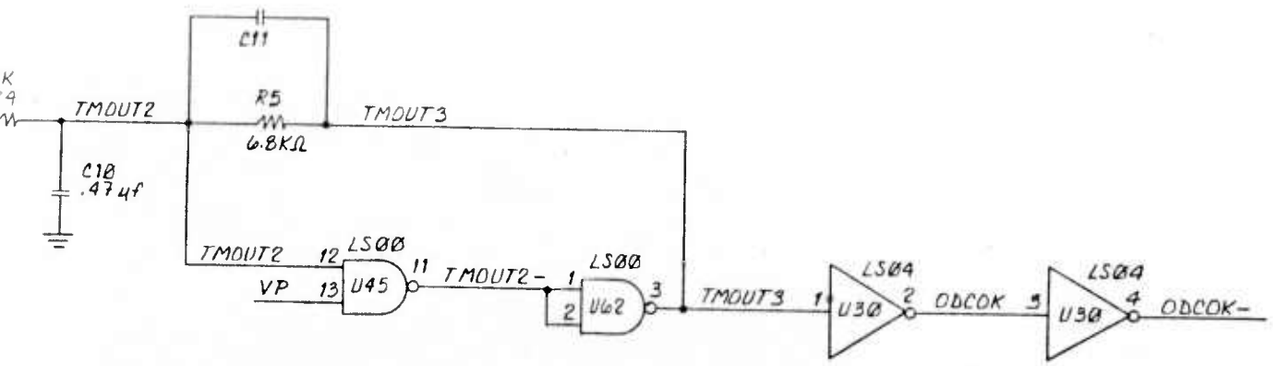
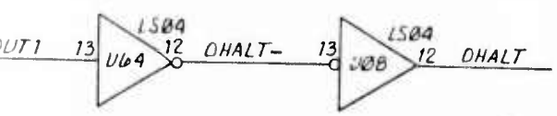




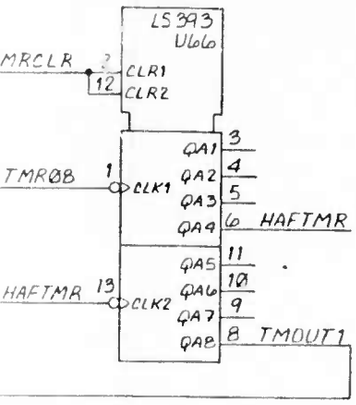
ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

CONTRACT NO
APPROVALS
DRAWN Middell
CHECKED Lewis
ISSUED
MATERIAL
FINISH
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING

DWG NO 2600466 SH 5 REV F

ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SH 1		



DWG NO 2600466 SH 5 REV 6

WATCH DOG TIMER

PARTS LIST

ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

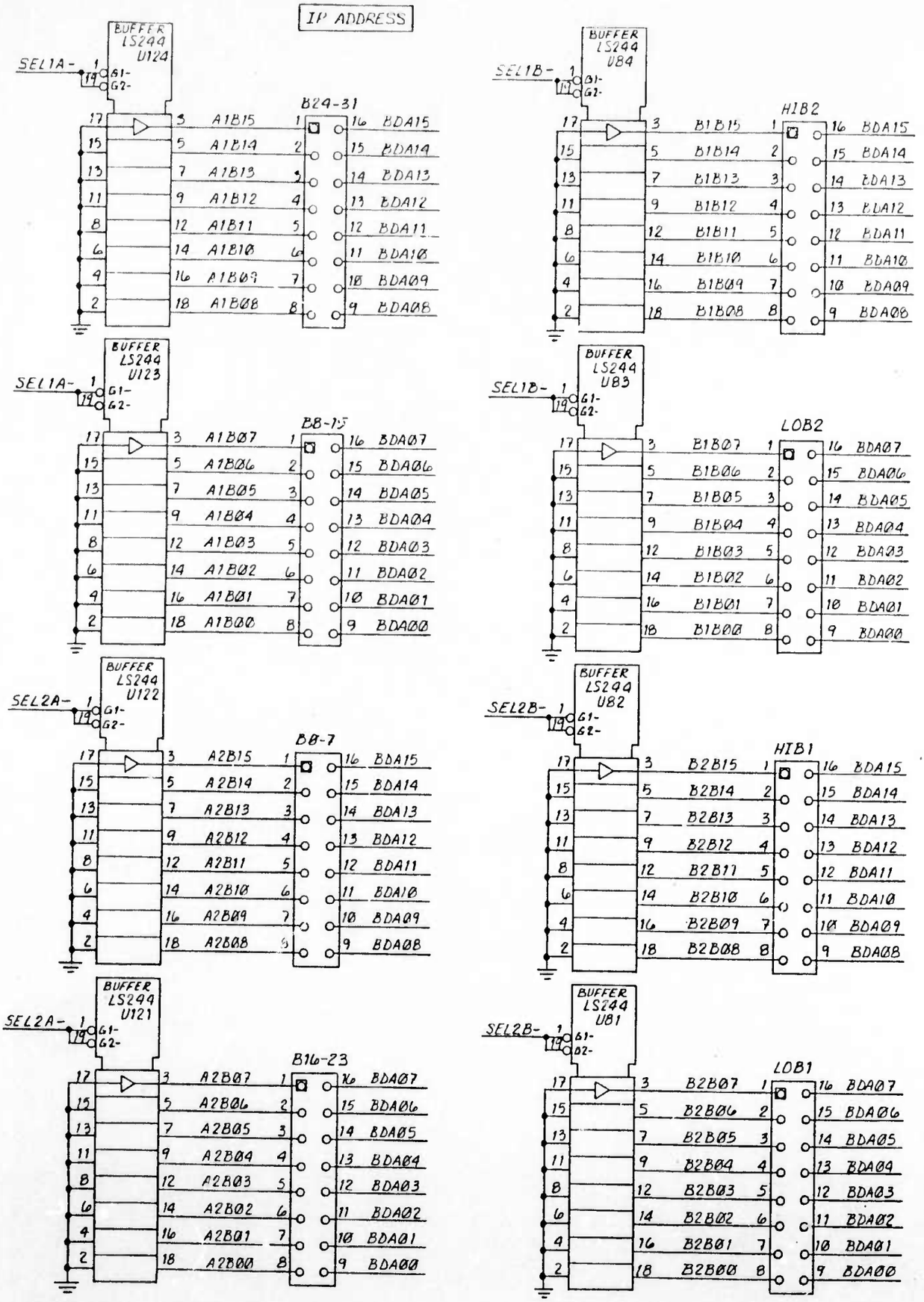
APPROVALS	DATE
DRAWN W. Liddell	28Sept82
CHECKED M. Lipka	10/4/82
ISSUED	

ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

LOGIC DIAGRAM
ROBUSTNESS II MOD

SIZE D | FSCM NO. 61550 | DWG NO. 2600466 | REV 6

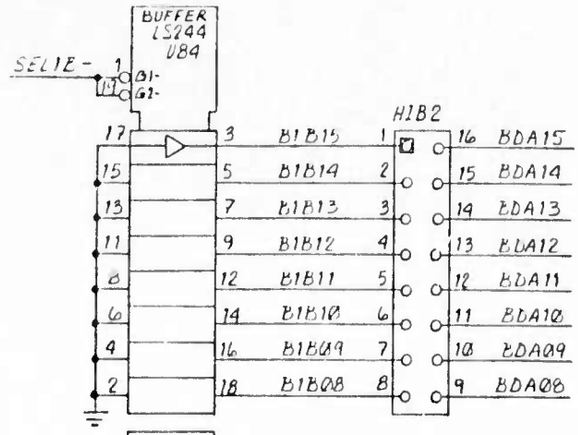
SCALE NONE | SHEET 5 OF 6

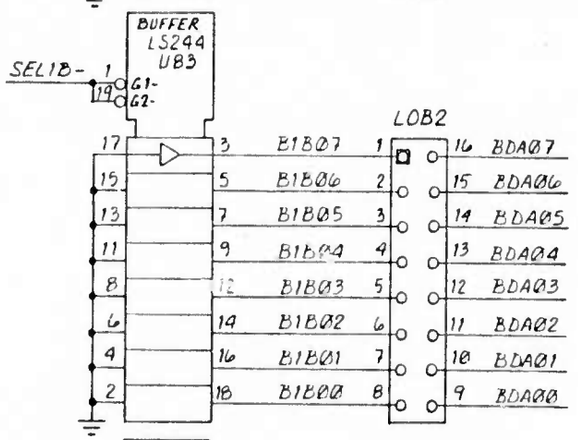


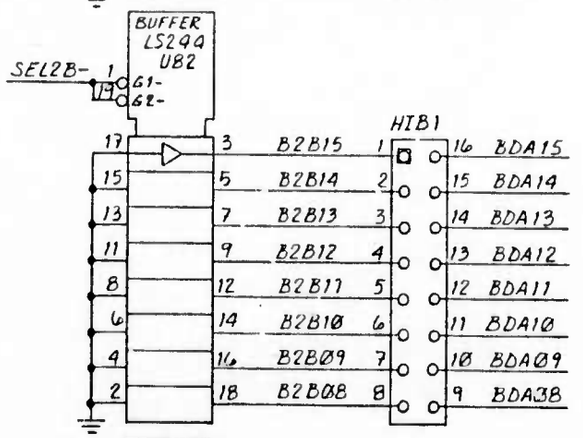
DWG NO 2

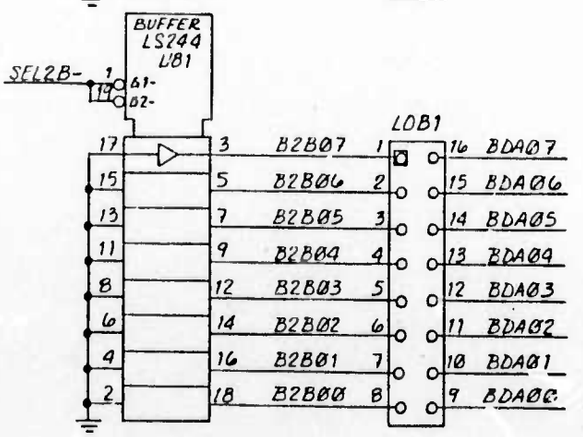
ZONE | REV

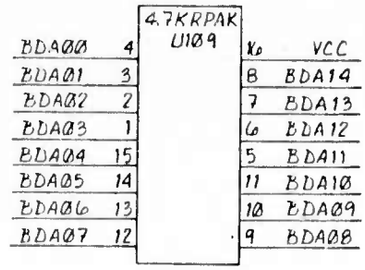
DDRESS

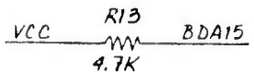


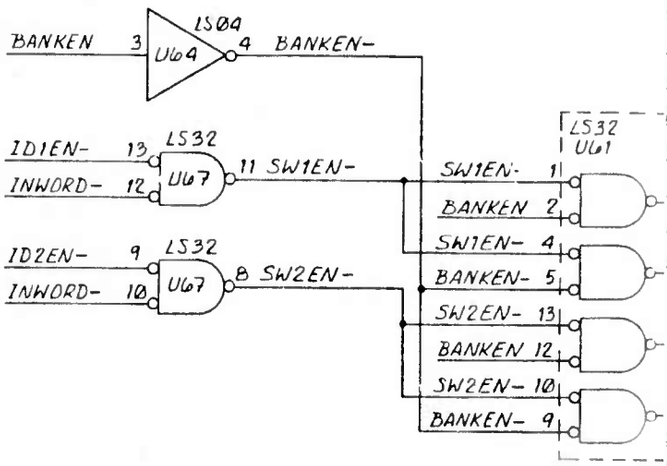












ITEM NO	QTY REQD	BOM NO	PART OR IDENTIFYING NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS

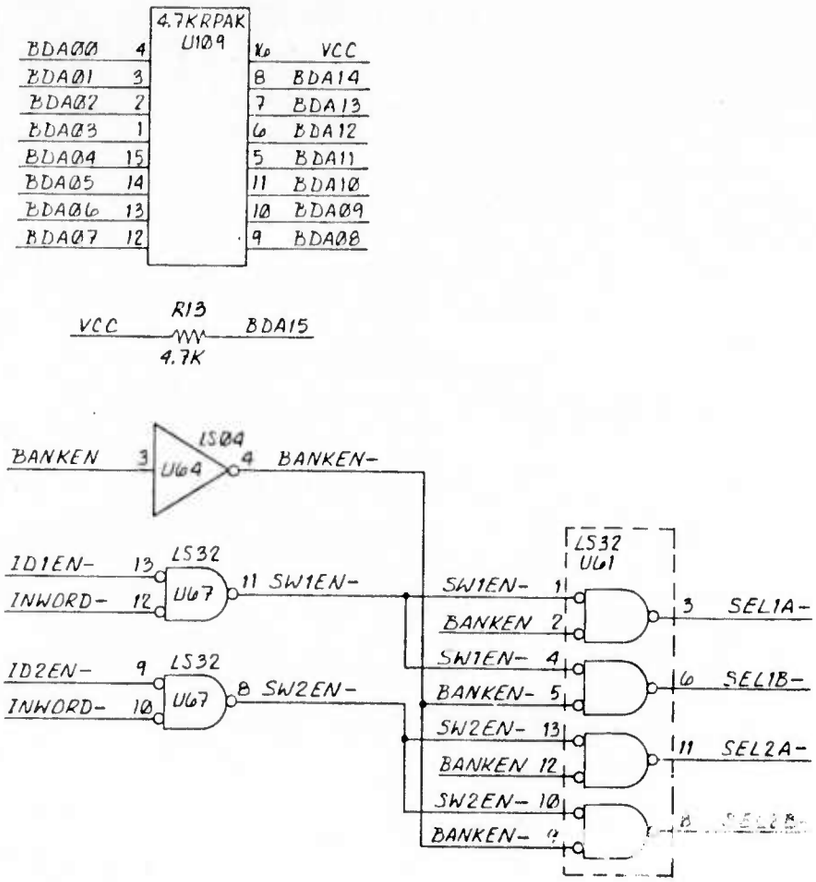
DRAWN WEDDELL

CHECKED

ISSUED

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SH 1		



SWITCH REGISTERS

ITEM NO	QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO

	APPROVALS	DATE
DRAWN	WEDDELL	5-18-82
CHECKED	M Lurch	1-4-82
ISSUED		

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

©

ASSOCIATED COMPUTER CONSULTANTS
Santa Barbara, California 93101

LOGIC DIAGRAM ROBUSTNESS II MOD

SIZE D | FSCM NO 61550 | DWG. NO. 2600466 | REV 6

SCALE NONE | SHEET 6 OF 6

DWG NO 2600466 SHT 6 REV 6

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: 002	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE *(and Subtitle)*: ROBUSTNESS II FINAL DOCUMENTATION "ROBUSTNESS II MAINTENANCE MANUAL"	5. TYPE OF REPORT & PERIOD COVERED: Final Documentation
6. PERFORMING ORG. REPORT NUMBER: ACC-25-002 (ROBUSTII-MM-V001)	
7. AUTHOR(s): Shawn Miner (805)963-9431	8. CONTRACT OR GRANT NUMBER(s): MDA903-82-C-0478
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ROBUSTNESS II LSI-11/23 ROBUSTNESS MODULE BOOT MODULE LSI-11 BOOT

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

For the enhanced version of the Robustness Module, the Robustness II, this document provides: installation, programming, and maintenance information in the form of text; assembly drawings; socket and pin location diagrams for memory and option selection; schematic diagrams and parts list. The ROBUSTNESS II is used in the LSI Network gateway; and provides: 128 Word (16-Bit) BOOT ROM, space for 8k Words of EPROM, Watch Dog Timing, Elapsed Time Counter (31 bits at 10KHz Clock Rate), -- continued on opposite side

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